Design of An Integrated High Voltage Controller in CMOS-Technology for Tunable Multiport Microwave Devices

Vom Fachbereich 18
Elektro- und Informationstechnik Institut für Datentechnik
der Technischen Universität Darmstadt
zur Erlangung des akademischen Grades eines
Doktor-Ingenieurs (Dr.-Ing.)
genehmigte Dissertation

von

M.Sc.
Jing Ning
geboren am 04. April 1983
in Beijing, China

Referent: Prof. Dr.-Ing. Klaus Hofmann
Technische Universität Darmstadt

Korreferent: Prof. Dr.-Ing. Rolf Jakoby
Technische Universität Darmstadt

Tag der Einreichung: 25.09.2015
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Erklärung zur Dissertation

Hiermit versichere ich, die vorliegende Dissertation ohne Hilfe Dritter nur mit den angegebenen Quellen und Hilfsmitteln angefertigt zu haben. Alle Stellen, die aus Quellen entnommen wurden, sind als solche kenntlich gemacht. Diese Arbeit hat in gleicher oder ähnlicher Form noch keiner Prüfungsbehörde vorgelegen.

Darmstadt, den

Jing Ning

(Jing Ning)

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Darmstadt, September 2015

Jing Ning

Abstract

As portable devices are required to operate in different frequency bands and work under changing environment conditions, reconfigurable *RF* devices, which required high biasing voltages above $100\ V$, are used in *RF* frond-end to achieve the multi-bands functionality. The size and cost of discrete circuits are not acceptable for most hand-held devices. Thus, high voltage *ASIC*, which can be easily integrated and powered by a battery, is a better solution to provide the biasing voltage. High voltage *ASIC* design is a relatively new field in chip design. To support safe operation voltage above $100\ V$, sophisticated physical structures with multiple isolation layers, extra drain region and thick oxidation gate are used in high voltage technologies and result in worse performance than designs with low voltage technologies. Thus, chip size, cost, power consumption and performance become the biggest challenges of the proposed design.

In this dissertation, two high voltage *ASIC* designs used to provide the biasing voltage for tunable components in communication systems are proposed. These *ASICs* can operate with a high voltage power supply generated by an on-chip *DC-DC converter*. Both designs are simulated in Cadence, implemented in *AMS H35* and experimentally tested.

The first *ASIC* is 8-bits high voltage *DAC* designed in segmented architecture with a *Segmented Transistor Only DAC* and a high voltage *Miller-compensated Amplifier* to boost up the output of the low voltage *DAC* to the expected high voltage. It can provide the biasing voltage for tunable devices up to $115\ V$ with 256 voltage steps. The *INL* and *DNL* of the *HV DAC* are $0.48\,LSB$ and $0.38\,LSB$, respectively. The power consumption is $18\,mW$, and the chip size is $3.5\ mm^2$.

The second *ASIC* is a high voltage controller mainly consisting of 16 *HV DACs* and a simple digital controller. Each *HV DAC* consists of a *Current Steering DAC* and a high voltage *Miller-compensated Amplifier*. It is able to provide 16 individual voltages up to $120\ V$ for different channels of antenna arrays in communication systems. Because of the process and mismatch variations, each *HV DAC* on the same chip has different performance. Based on the experimental test, the worst *INL* and *DNL* of the *DACs* are $0.98\ LSB$ and $0.52\ LSB$, respectively. The total power consumption is $120\ mW$, and the chip size is $10.88\ mm^2$.

Besides the experimental test, a demonstrator is built to prove the feasibility to use *HV ASICs* to apply the required biasing voltage of the tunable components in portable devices. The measurement result is also presented in this dissertation.

Kurzfassung

Die mobile Geräte arbeiten oft in unterschiedlichen Frequenzbereichen und ständig wechselnden Umgebungen. Um in *HF* Front-End die Multi-band Funktionalität zu realisieren, benötigen die Geräte rekonfiguierbare Hochfrequenz-Module mit einer Biasspannung über $100\ V$. Jedoch sind die diskrete Schaltungen wegen deren Größe nicht integrierbar in mobilen Geräten. Weiterhin machen die hohe Herstellungskosten für den Einsatz der diskreten Schlatungen in mobilen Geräten unmöglich. Die Hochspannung *ASICs* können mit Batterie betreiben werden. Wegen ihren kleineren Baugrößen sind die Hochspannung *ASICs* Module die beste Lösung für Biasspannungsversorgung in mobilen Geräten. Die Hochspannung *ASIC* ist ein Neuling im Bereich Chip Entwurf. Im Vergleich zu Niederspannung *ASIC* büßt die Performance der Hochspannung *ASIC* bei Spannungsversorgung über $100\ V$ aufgrund ihren komplexen physikalischen Strukturen ein. Die Baugröße, die Herstellungskosten, der Energieverbrauch und die Performance sind die größte Herausforderungen bei der Entwicklung des vorliegden Schaltungsentwurfs.

In dieser Arbeit werden zwei Hochspannung *ASIC* Entwrfe für die Biasspannungsversorgung der rekonfiguierbaren Komponenten in Kommunikationssystemen vorgestellt. Beide *ASICs* können mit einer Hochspannungsversorgung von einem *On-Chip DC-DC Wandler* betrieben werden. Beide Schaltungen werden zuerst in Cadence simuliert. Darauf folgt die Implementierung in *AMS H35* und Praxistest.

Die erste *ASIC* Schaltung ist eine 8-bits Hochspannung *DAC* und besteht aus einem *Segmented Transistor Only DAC* und einem Hochspannung *Miller-compensated Verstärker*. Die maximale Vorsorgungspannung betrgät maximal $115\ V$ und ist stufenweise in 256 Schritten einstellbar. Die *INL* und *DNL* der *HV DAC* sind jeweils $0.48\ LSB$ und $0.38\ LSB$. Der Energieverbrauch ist $18\ mW$. Die Größe des Chips beträgt $3.5\ mm^2$.

Die zweite *ASIC* Schaltung besteht aus 16 *HV DACs* und einem Digitalregler. Jede Hochspannung *DAC* besteht auch ein *Current Steering DAC* und ein Hochspannung *Miller-compensated Verstärker*. Diese Schaltung liefert 16 kanalige Vorsorgungsspannung bis maximal 120V für Antennen Array in Kommunikationssystem. Aufgrund der Herstellungsabweichung haben die *HV DACs* unterschiedliche Leistungsfähigkeiten. Im Versuch weisen die *DACs* beim schlechten Bedingungen eine *INL* und *DNL* von $0.98\ LSB$ und $0.52\ LSB$ vor. Der Energieverbrauch ist $120\ mW$. Die Größe des Chips beträgt $10.88\ mm^2$

Um die Einsatztauglichkeit der Schaltung zu testen, werden die *HV ASICs* für die Spannungsversorgung der rekonfiguierbaren Modulen in mobilen Geräten eingebaut.

Die Versuchsergebnisse werden ebenfalls in dieser Arbeit aufgeführt.

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List of Abbreviations

ASIC	:	Application Specific Integrated Circuit
RA	:	Reconfigurable Antenna
UMTS	:	Universal Mobile Telecommunications System
WLAN	:	Wireless Local-area Network
WiMAX	:	Worldwide Interoperability for Microwave Access
RF	:	Radio Frequency
MEMS	:	Microelectromechanical System
DAC	:	Digital to Analog Converter
ADC	:	Analog to Digital Converter
FPGA	:	Field Programmable Gate Array
CMOS	:	Complementary Metaloxidesemiconductor
DMOS	:	Double-diffused Metal-oxide-semiconductor
HV	:	High Voltage
HV CAP	:	High Voltage Capacitor
SoC	:	System on Chip
BCD	:	BIPOLAR-CMOS-DMOS
DEMOS	:	Drain Extended MOS
DDDMOS	:	Double Diffused Drain MOS
LDMOS	:	Lateral Drain MOS
LCD	:	Liquid-crystal Display
RESURF	:	Reduced Surface Field
MOSFET	:	Metaloxidesemiconductor Field-effect Transistor
SOI	:	Silicon on Isolator
MIM	:	Metal Insulator Metal
ERC	:	Electrical Rule Check
DRC	:	Design Rule Check
DSP	:	Digital Signal Processor
MSB	:	Most Significant Bit
LSB	:	Least Significant Bit

INL	:	Integral Non Linearity
DNL	:	Differential Non Linearity
SNR	:	Signal-to-Noise Ratio
SFDR	:	Spurious Free Dynamic Range
ESD	:	Electrostatic Discharge
SOAC	:	Safe Operation Area Check
TMN	:	Tunable Matching Network
VCSEL		Vertical-cavity Surface-emitting Laser

Chapter 1

Introduction and Overview

Contents

1.1 Background

Integration and miniaturization of the application specific integrated circuits (*ASICs*) play an important role in performance improvement and cost reduction of electronic systems. According to Moore's Law, the number of transistors in a dense integrated circuit doubles approximately every 18 months during the past decades. [Moo] The first systems based on the upcoming Core M processor, which will be manufactured on Intel's 14nm technology, will be available in Q4 2014. [Int] However, due to the technology limitation, Moore's Law is becoming more challenging and probably comes to the end in the foreseeable future. The transistor scaling is far more suitable for implementation of low voltage *ASICs*, especially for digital circuits. Owning to physical limitations, high voltage *ASICs* do not follow Moore's Law in the past decades. Nowadays high voltage *ASICs* designers are more concerned with More-than-Moore, which has been used in different application areas such as sensors, actuators and *RF* devices in communication systems.

1.2 Motivations

The research of tunable devices such as universal radio frequency transceivers used in mobile and satellite communications has gained attraction within the last years. To fulfill the requirement of multi-system operation, modern devices with tunable components (e.g. reconfigurable antenna(*RA*) arrays) are useful to operate in different frequency bands and support large number of standards(e.g., *UMTS*, *Bluetooth*, *WLAN*, *WiMAX*). By using a chain of RF components, as shown in Fig. 1.1, will greatly increase the hardware complexity and power consumption of the system. Thus, reduction of the complicated parallel structure of RF-frontends is a requirement to improve the multi-functionality and compatibility of the devices.

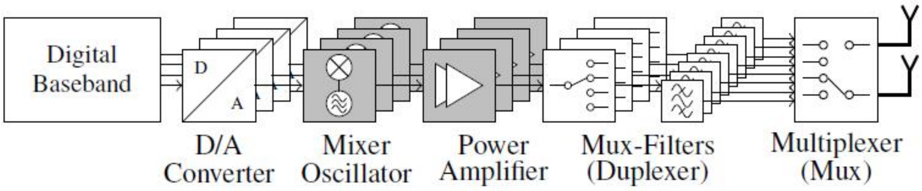


Fig. 1.1: Transmitter chains of multiband RF-frontend [GRMS+13]

To overcome this challenge, one of the most attractive solution to achieve reconfigurability for multi-functional operation and variable environmental conditions in one device is to use tunable microwave components by applying semiconductor, microelectromechanical systems(*MEMS*) and functional materials, such as ferroelectrics and liquid crystal, as shown in Fig. 1.2.

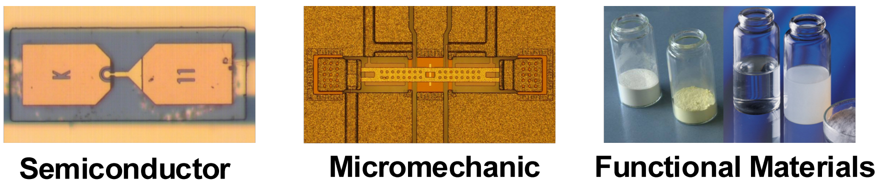


Fig. 1.2: Materials used to implement tunable microwave components

These components change its characteristics to reconfigure the architecture and to offer multiple services within the same *RF* chain or to compensate any emerging mismatch under changing condition [GRMZ+14]. Most methods to realize controllable components require relative high biasing voltage. Since there is a popular trend towards increasing integration density and decreasing cost of the communication devices with tunable components, the high voltage requirement results in a big challenge to integrate high voltage generator and controller into portable devices.

Comparing with others [WBJL11,HCA+08,BP+13,JSMW04], functional materials have higher tunability and linearity. Therefore, many researches [MSJ11] [GZM+08] [MSZJ10] focus on the implementation of tunable devices by applying functional materials(e.g. functional ceramics, liquid crystal, electroluminescence). Because of having tuning voltage dependent electromagnetic properties, these materials require DC or pulsed AC voltages beyond $100\ V$. Therefore, an integrated high voltage controller with multi-output which can provide different voltages from $0\ V$ to $120\ V$ is required by the universal radio front-end as shown in Fig. 1.3.

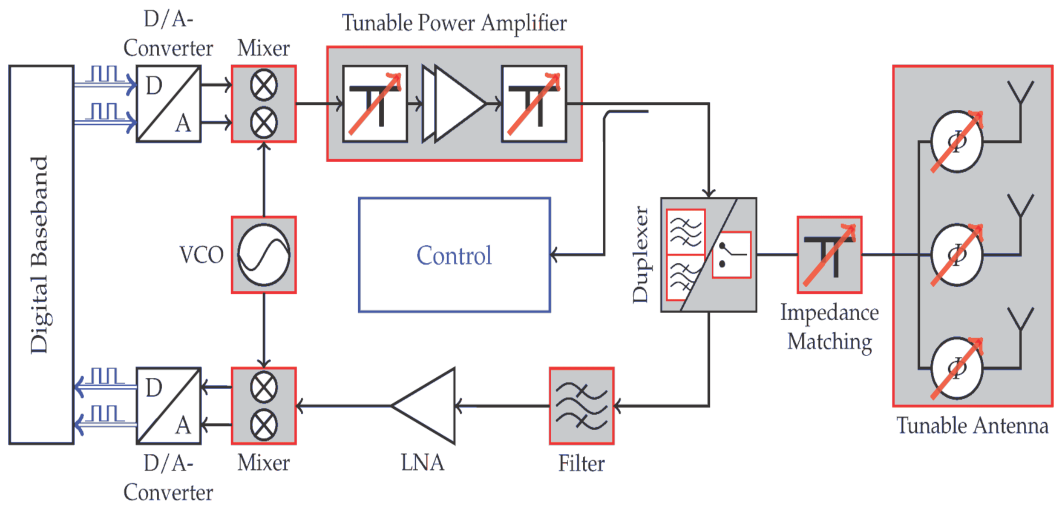


Fig. 1.3: Universal Radio Front-end

If the high voltage controller can be implemented on chip, the cost and complexity of these communication systems will be greatly reduced. Fortunately, more and more *CMOS* and *DMOS* technologies (e.g. *AMS H35*, *XFAB XDH10*, *XFAB XU035*) can provide high safe operating voltages above $100\ V$. These new high voltage technologies dramatically improve the feasibility to implement such a required high voltage controller on chip.

1.3 Research Objectives

The main task of this dissertation is to design and implement an integrated high voltage controller in *CMOS* technology to drive tunable antenna in communication devices. To fulfill the high voltage requirement of functional materials, it should able to provide voltages from $0\ V$ to $120\ V$ with voltage step of $0.45\ V$.

Since the high voltage power supply in portable devices has to be generated by *CMOS* charge pump from nominal batteries [SH12], the load current of the high voltage power is quite limited. For integrating the charge pump and the high voltage controller into portable devices, the current consumption of the high voltage controller must be sufficient low. Moreover, the characteristics such as leakage current, threshold voltage and switching speed of high voltage devices are worse than low voltage ones caused by their sophisticated physical structures. Thus, it is also necessary to overcome the worse physical characteristics to achieve expected circuit performances. Furthermore, due to the relative large size of the high voltage devices, reduction of the chip area becomes another main challenge.

In summary, the main research goal is to implement an integrated high voltage controller with multiple *DACs*, which can be integrated into portable devices, in *HV CMOS* technology in a reasonable size.

1.4 Thesis Outline

The remaining chapters are briefly described in the following.

- *Chapter 2*: This chapter briefly introduces the high voltage technologies, the special physical structure and characteristics of high voltage devices. The available high voltage *DAC* designs in different high voltage technologies are introduced as well. Furthermore, the general design methodology and challenges are mentioned. The feasibility to design an integrated *CMOS* high voltage controller, which can fulfill the requirement of our application has been discussed as well.

- *Chapter 3*: This chapter proposes a high voltage digital to analog converter with a single output fabricated in *AMS H35 CMOS* technology. It can provide output voltage from $0\ V$ to $115\ V$ with voltage step of $0.45\ V$. The *HV DAC* mainly consists of a low voltage *Segmented Transistor Only DAC* and a high voltage *Miller-compensated Amplifier*. The advantages and disadvantages of the proposed architecture are discussed. Moreover, the design and the implementation of the main parts are described in details. At last, both simulation and experimental results are presented and discussed.

- *Chapter 4*: This chapter proposes an improved high voltage controller consists of 16 *HV DAC* and a simple digital controller. In this new design, the output voltage swing is extended to $0 - 120\ V$(maximum operating voltage in *AMS H35)*. Furthermore, comparing with 16 single output *HV DACs*, the size of the new chip is also dramatically reduced. The implementation is also presented in details. To overcome the gain error and offset error caused by process and mismatch variations, a calibration method is discussed as well. In the last section, the simulation and experimental results are presented and discussed.

- *Chapter 5*: This chapter briefly introduces the highly requirement of high voltage *ASICs* in different application areas such as communication system, medical equipment and car system. After introducing the background of the application, a demonstrator for proving the feasibility to integrate *HV ASICs* into communication systems is presented. Measurement results of the demonstrator, further discussion and a short summary are presented in the chapter as well.

- *Chapter 6*: The challenges and contributions of the thesis are summarized in this chapter. In the end, further works to improve the performance and to reuse the proposed design in other applications are briefly introduced.

Chapter 2

Integrated High Voltage DAC with CMOS Technologies

Contents

2.1 High Voltage CMOS Technologies

In *CMOS* design domain, any voltage above $5\ V$ is thought of as high voltage. According to rapidly increased number of transistors on chip and requirement of the power consumption, the maximum supply voltage has to be decreased to achieve high speed and low power specifications. Thus, most *ASICs* can not be used in applications, which require high voltage. To fill this gap, many high voltage technologies such as *AMS H18* [H1814], *AMS H35* [H3514], *XFAB XH018* [XH014], *XFAB XU035* [XU014] and *XFAB XDH10* [XDH14]are released to provide high operation voltages. Nowadays, the development of high voltage technology greatly increase the feasibility to design high voltage *ASICs* and to integrate them into portable devices.

Depending on various requirements of the applications, different high voltage technologies are chosen to design high voltage circuits. For power applications, *BCD* technologies are more popular to be used because of the high current requirement. *CMOS* technologies are more dedicated to be used in applications which require high voltage and low current. According to our specific application, this work only focus on high voltage *CMOS* technologies.

2.1.1 Structure of High Voltage Devices

In order to provide high operation voltage, special physical structures are required for high voltage devices. Normally, high voltage MOS devices can be implemented as *Drain Extended MOS* (*DEMOS*), *Double Diffused MOS* (*DMOS*), *Double Diffused Drain MOS* (*DDDMOS*) or *Lateral Drain MOS* (*LDMOS*). In this section, the most popular high voltage devices (*DDDMOS* and *LDMOS*) are briefly introduced. Both can be integrated into *CMOS* process by adding extra layers [HHY+13].

DDDMOS devices are widely used in applications requiring high voltage above $20\ V$ such as drive circuits for *LCD* display. Compared with *LDMOS*, it can be easily integrated into *CMOS* process, and the cost is much lower. However, the operation voltage is relatively low. In industry, other applications such as integrated power circuit for automotive and *RF* applications require higher voltage [Lar03, BRB+09]. In these fields, *LDMOS* devices with higher operation voltage above $100\ V$ have been most frequently used.

Fig. 2.1 shows the structure of *DDDMOS*. In this structure, an extra drain is implemented by adding a light n-type dopant area between the drain and the channel. This structure can be seemed as a standard *MOS* transistor plus an extra resistance whose value depends on the doping concentration and the scaling of the extra drain area. Thus, the voltage on the effective channel is decreased by adding this on-resistance of the high voltage transistor.

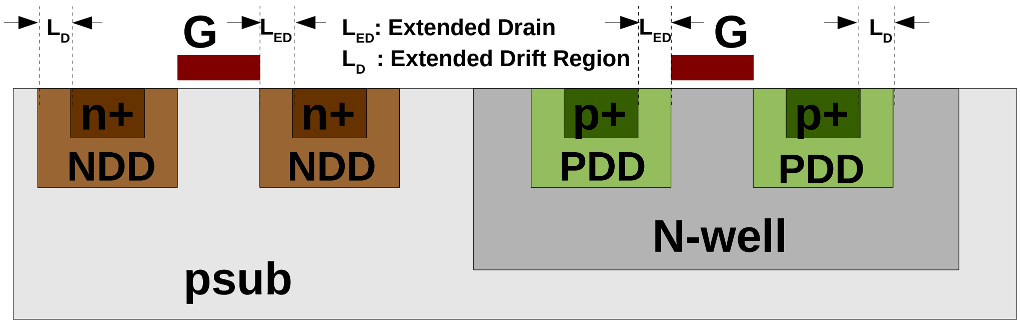


Fig. 2.1: The cross section of Double Diffused Drain MOSFET

Fig.2.2 shows the cross section of *LDMOS*. By using *RESURF* Technology [AV79], its breakdown voltage is dominated by the vertical breakdown voltage between the substrate and the light dopant N-Well. In this structure, the diode consists of two parts, one horizontal PN junction and one vertical PN junction. Different from low voltage *MOSFET*, with thin epitaxial N-well (N^-) the depletion layer of P^+N is reinforced by the horizontal PN junction between the epitaxial layer and the substrate. Thus, the depletion layer stretches along the surface over a longer distance, and the electric field at the surface greatly decreases. Above a certain thickness of the epitaxial layer, the electric field at the surface will not exceed the critical point even at high voltages, and the break down voltage of the device only depends on the vertical PN junction.

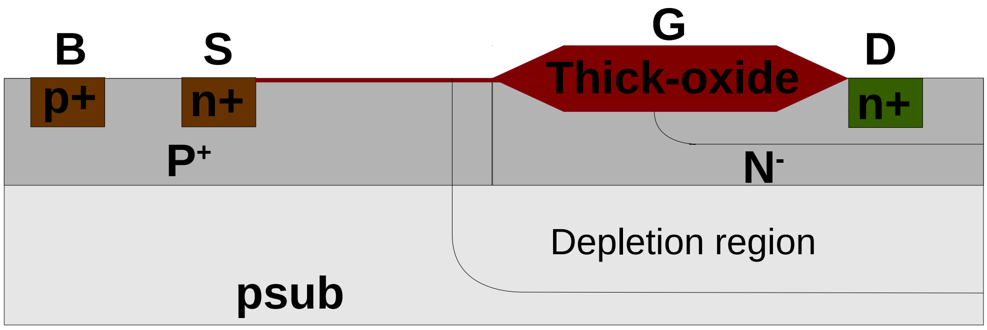


Fig. 2.2: The cross section of Lateral Double Diffused MOSFET

2.1.2 Technology Selection

Due to their sophisticated physical structures, the scaling of high voltage devices is much larger compared to standard low voltage ones. As shown in Fig. 2.1 and Fig. 2.2, the critical parameter at the transistor level is the length of the extended drain area. Since the operation voltage scale depends on the scaling and the doping concentration of the extra epitaxial layer, the maximum operation voltage and the scaling of the transistors are the trade-off. To optimize the area efficiency, all specifications including maximum voltage, frequency, area and cost have to be taken into account to select a proper technology.

Though several high voltage technologies are available, only a few can achieve the required high voltage range of our application above $100\ V$. In those processes, *XDH10* and *XU035* provide $650\ V$ *DMOS* transistors and $750\ V$ bipolar transistors, respectively. *XDH10* is a silicon on isolator (SOI) process which is compatible with *CMOS* technology. As shown is Fig. 2.3 a trench is required for each high voltage device to isolate from neighbors and to decrease the leakage current. Compared with AMS H35 as shown in Fig. 2.4, the scaling of the high voltage transistors, which are physically isolated, is not acceptable for our application. *XU035* is a *BCD-like* process which has high voltage *CMOS* transistors with long extended drain areas. Therefore, its scaling is much larger than *AMS H35*.

Considering the voltage range of our application, chip area and the cost, *AMS H35* is

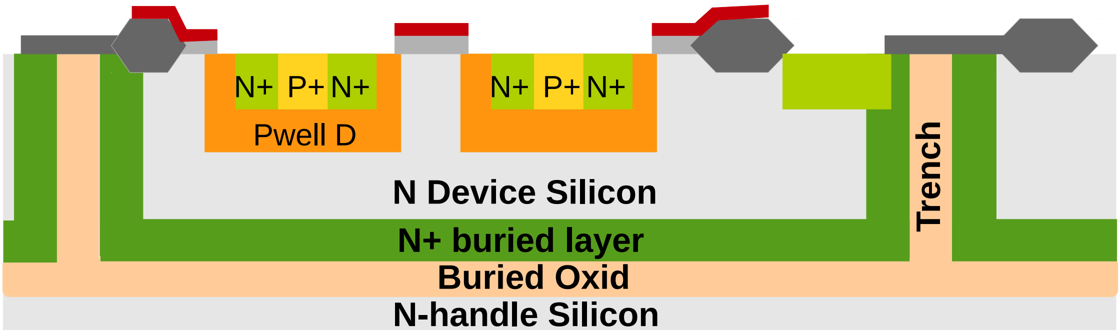


Fig. 2.3: XFAB10 core cross section

selected to implement our design. In this technology, high voltage devices are available to operate safely with high voltage up to $120\ V$.

Fig. 2.4 shows the structure of $120\ V$ *NMOS* transistor in this technology. The maximum voltage($120\ V$) between drain and source is achieved by using *LDMOS* technique. In this technology, three gate oxidation layers with different thickness are available. The maximum gate source voltage(V_{GS}) is $20\,V$ while using the thickest oxidation layer. Compared to devices in low voltage technologies, more isolation layers exit in the structure. The complicated physical structure results in more parasitic elements in and between the layers. It is the main reason that the characteristics of these devices are worse than low voltage ones. To avoid latch up effect and guarantee the isolation between neighbor blocks in the circuit, guard ring is required for each high voltage device as shown in Fig. 2.4. It obviously brings about larger size of the high voltage devices than low voltage ones.

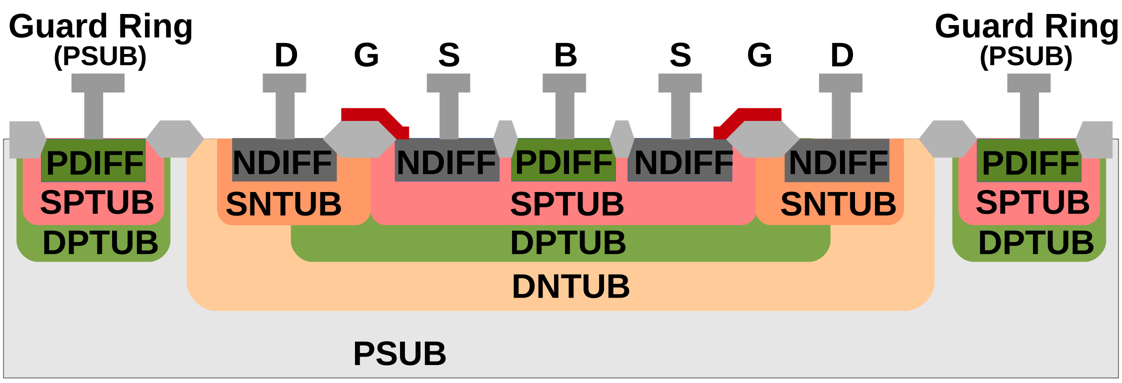


Fig. 2.4: The cross section of $120V$ high voltage NMOS transistors

High voltage capacitors are also available in *AMS H35*. Fig. 2.5 shows the structure of $120\ V$ capacitors in this technology. The low capacitance density of this sandwich capacitor leads to a large area consumed by *HV CAPs* required by the application. Since the operating voltage of other capacitors is limited to $50V$ [Doc14b,Doc14a], the sandwich capacitors can not be replaced in this high voltage circuit requiring $120\,V$.

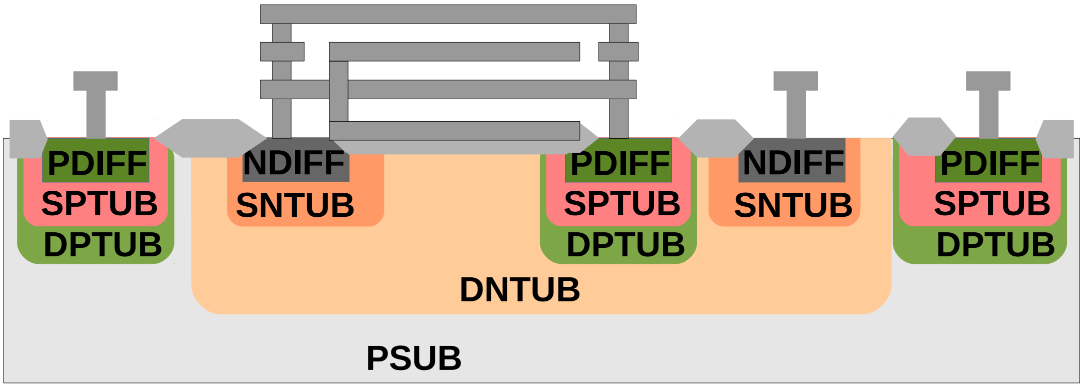


Fig. 2.5: The cross section of $120\,V$ high voltage capacitors

In this technology, high voltage devices are compatible with conventional low voltage devices. Design low voltage parts of the chip by using low voltage transistor and capacitors such as polysilicon capacitors and *MIM* capacitors will dramatically decrease the area and the cost. Furthermore, the power consumption can be greatly reduced by using low voltage part as well. It will make the *ASIC* solution more suitable to portable devices.

2.2 State of the Art

To drive reconfigurable microwave devices, either external DC power supply or discrete circuit are used to apply high voltage to tunable materials. Up to now, such an integrated high voltage controller is not available for this special application. However, high voltage *DACs* up to $300V$ have been designed for other applications [BJ11,YCZ+95,HC12,SMP05, Nay83].

2.2.1 High Voltage R2R Digital to Analog Converter

In Zuguang Yu's work [YCZ+95], a 11-bits compatible *HV DAC* has been implemented for audio and video telecommunications. It consists of a current limitation circuit, a R2R network and a switch array as shown in Fig.2.6, and can provide high output voltage up to $40\,V$.

The conventional high resolution resistor-string *DAC* requires large resistor ratios which results in non-linearity because of the process and mismatch variations during fabrication. Compared to it, the structure of *R2R DAC* being composed of resistors with only two precision values(R and 2R)as shown in Fig. 2.7 can overcome the mismatch is-

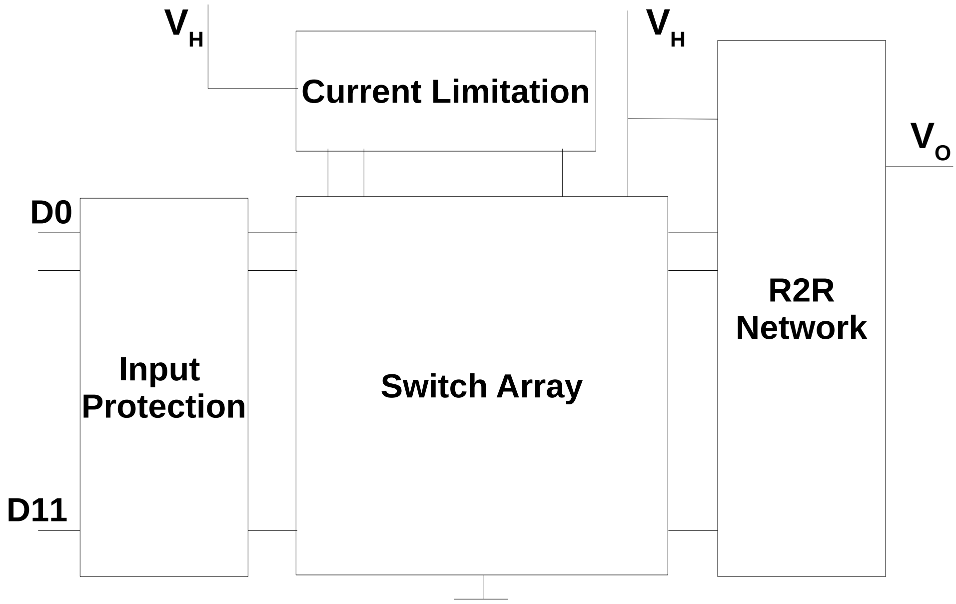


Fig. 2.6: R2R high voltage DAC for audio and video telecommunications

sue and achieve better linearity as shown in Fig. 2.7. An N-bits *DAC* requires only 2N resistors. It was first proposed by D. B. Smith [Smi53].

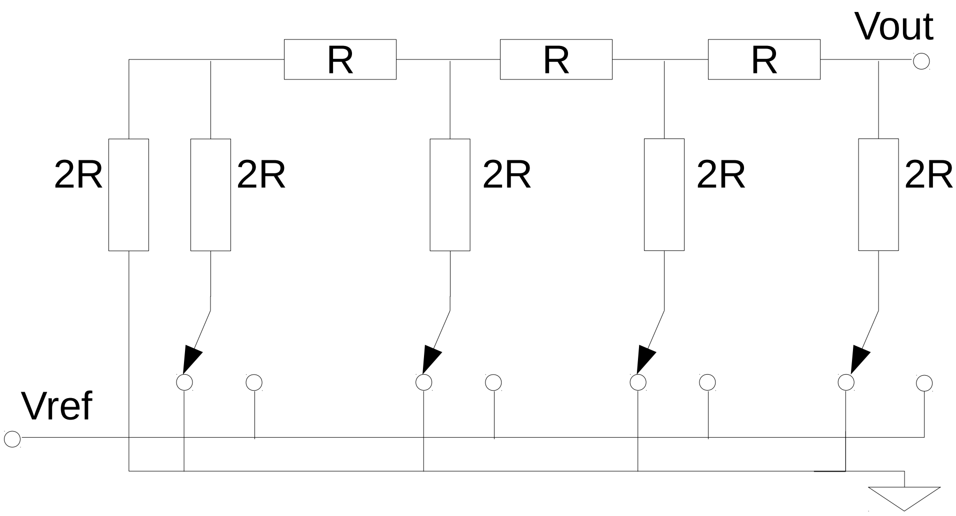


Fig. 2.7: R2R DAC proposed by D. B. Smith

Besides the discussed performances, the cost has to be taken into account as well. Unfortunately, the size of R2R topology is relatively larger than current steering *DAC*, which is composed of transistors. In this work, the chip size is $5.024 * 3.898\ mm^2$.

2.2.2 High Voltage Current Steering Digital to Analog Converter

In Johan Borg's work [BJ11], a 8-bits high voltage digital to analog converter has been fabricated in $0.35\mu m$ *CMOS* technology for an ultrasonic measurement application. An ultrasonic device typically converts an excitation into an acoustic wave and back into electrical signal after it has interacted with the sample. This work presents the first published integrated ultrasonic transducer interface circuit as shown in Fig. 2.8. A transducer T is driven by DAC1 which provides V_{pp} of $40V$. The received electrical signal converted from acoustic wave is propagated through a high voltage switch (SW2) to an external *ADC*. The other high voltage *DAC* is used to calibrate the signal path by performing measurements on an external reference impedance Z_r. The *FPGA* in the system is used to generate the clock and data to drive the high voltage *DAC*.

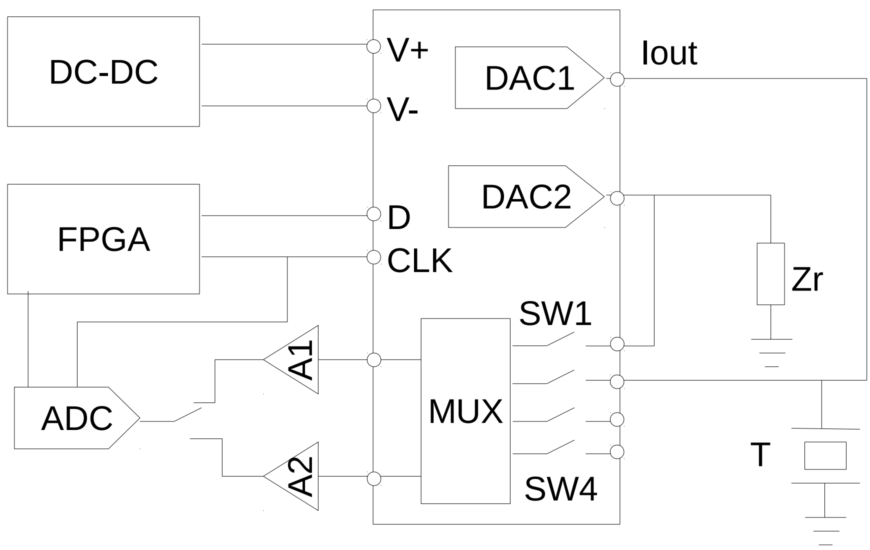


Fig. 2.8: Ultrasonic measurement system proposed by Johan Borg

The high voltage *DACs* use 63 unary high voltage current sources controlled by 6-bits thermometer code and 2-bits binary weighted code. Binary output current is generated by a sink or a source *DAC* consisting of high voltage *NMOS* transistors and *PMOS* transistors, respectively, as shown in Fig .2.9.

Compared with R2R topology, this proposed *DAC* provides a higher output impedance and consumes smaller area. It operates with $+25\ V$ and $-25\ V$ power supply and can provide output current of $400\ mA$ with output voltage swing of $40V_{pp}$. The chip size is $3.7 * 2.2\ mm^2$. Since the whole circuit is powered by high voltage power supply, it consumes much current from high voltage power supply. Because of the output current limitation of integrated *DC-DC converter*, it is not suitable for mobile devices.

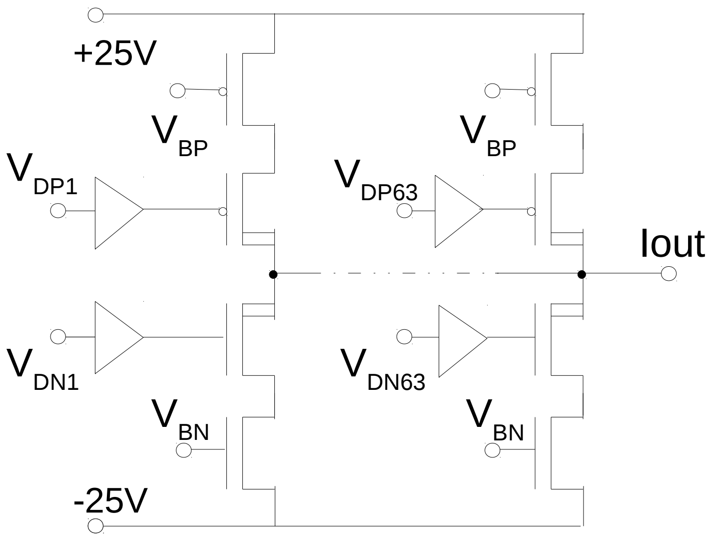


Fig. 2.9: Unary current source of sink and source DACs

2.2.3 High Voltage Digital to Analog Converter with High Voltage Driver

To save power consumption and to decrease chip area, some researches focus on the architecture composed of a low voltage *DAC* and a high voltage driver.

In Ya-Hsin Hsueh's work [HC12], a high voltage digital to analog converter has been designed by using *TSMC* $0.25\ \mu m$ *BCD* Process for medical applications. This 10-bits *DAC* can provide output voltage up to $60\ V$. The goal of this work is to consume smaller area as achieving the same function. Thus, the circuit was segmented into two parts, a low voltage current mode *DAC* and a high voltage driver powered by $5\ V$ and $60\ V$, respectively, as shown in Fig. 2.10.

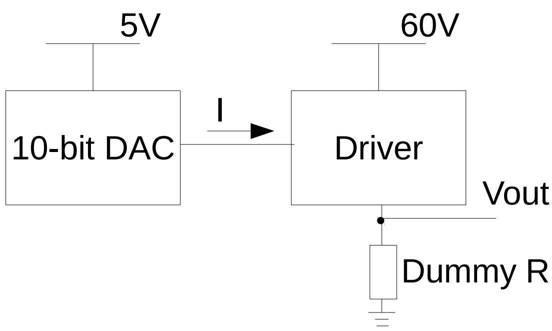


Fig. 2.10: Structure of the high voltage DAC proposed by Ya-Hsin Hsueh

The low voltage *DAC* is built with a conventional current mode architecture as shown in Fig. 2.9 while replacing the high voltage transistors in Johan Borg's work [BJ11] with low voltage ones. To achieve the high voltage function, Wilson current mirror [Wil68] is used to build the high voltage driver as shown in Fig. 2.11.

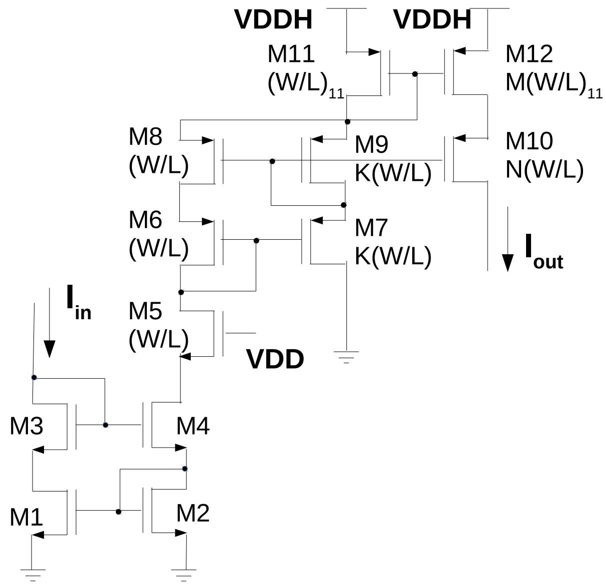


Fig. 2.11: Structure of the high voltage driver

This high voltage driver consists of two current mirrors. $M1$ to $M4$ compose a modified Wilson current mirror used to change the current direction. $M5$ is used to reduce the discrepancy between input and output current caused by different drain source voltages. Moreover, the drain voltage pressure is also reduced by using $M5$. $M6$ to $M12$ compose a input current amplifier, whose structure is similar to a cascade current source. The size of the transistors are calculated by using the following equation.

$$N = M * (K + 1) \tag{2.1}$$

This work applied Hspice for simulation. Based on simulation result, the maximum output current and voltage are $100\ mA$ and $50\ V$. The maximum *DNL* and *INL* are $-0.03\ LSB$ and $-0.28\ LSB$, respectively. The layout size is only $1.9 * 1.541\ mm^2$, much smaller than the mentioned work in section 2.2.1.

Another high voltage *DAC* consisting of a low voltage —textitDAC and a high voltage driver has been proposed by Ehab Shoukry [SMP05]. In this work, a fully integrated high voltage *DAC* array is designed in *DALSA* Semiconductor's $0.8\,\mu m$ *CMOS/DMOS* technology for electro-optic(*EO*). This design is based on a current-steering structure and consists of 64 6-bits *HV DACs*. Being different from Ya-Hsin Hsueh's work, two approaches to implement a high voltage driver are discussed. Besides a similar current mirror, a high voltage amplifier used to boost up the output voltage is described as shown in Fig. 2.12.

In this amplifier, all transistors has to be high voltage transistors. Due to the limitation of maximum gate source voltage, the reference current circuits must have high voltage devices as well. Since the relatively large size of high voltage devices, the increased number of high voltage transistors will result in quickly increased area. Thus, it is not an

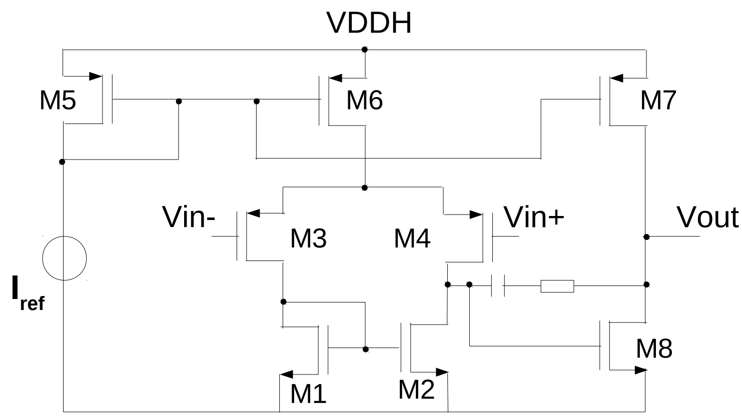


Fig. 2.12: Structure of the high voltage amplifier

optimal and feasible solution to implement a high voltage driver for mobile devices.

Unfortunately, the size and measurement result are not mentioned in the publication. According to the simulation result, the *DACs* operate from 0 to $300\ V$, having *DNL* of $-0.16\ LSB$ and *INL* of $-0.18\ LSB$.

2.3 High Voltage AISC Design Methodology

Being similar to standard *ASIC* design, the methodology of high voltage *ASIC* design contains four main categories: process selection, creating modules, circuit simulation and layout strategy. Due to large area and limited operating voltage of high voltage devices, high voltage *ASIC* design has more challenges. To achieve high voltage functions with acceptable area, conventional circuit architectures have to be modified to reduce the number of high voltage devices. Moreover, more *ERC* and *DRC* rules needs to be fulfilled to avoid latch-up and to reduce leakage current. Thus, circuit optimization and *ERC/DRC* are two additional topics needed to be discussed as well.

- *Process selection*: The first issue has to be considered in *ASIC* design is to select a proper process for the chip design and implementation. To select a proper technology, both price and required specifications of the system have to be taken into account. The most important technical requirements are safe operation voltage, parasitics, component tolerances and the integration density of the system. To achieve high operating voltages, the depth of the oxidation layer must be increased to avoid 'punch-off' of the gate caused by high voltages. To stand with high lateral voltage, the drain depletion region has to be extended as well. As a result, the feature size of the process increases as the safe operation voltage rising. Besides, extra isolation layers are required to decrease latch-up and to reduce leakage current. The required complex physical structures results in more parasitics, large size, more complicated process and hence relatively high cost of production. According to the available processes, high voltage operation above $100\ V$ is possible to be implemented on chip, but only in processes with feature sizes greater than 0.35 micrometer. To increase the integration density, the compatibility with low voltage devices is another important feature to be considered. In high voltage *ASIC* design, the chip is normally divided into a low voltage part and a high voltage part to reduce the area. Thus, low voltage devices should be provided by the selected process as well. Furthermore, for some applications, precision devices could be required to provide accurate outputs. As an example, the value of compensation capacitors and auto-zero capacitors in op-amp do not need to be accurate. In contrast, capacitors in digital to analog converters must be precisely matched to guarantee the resolution.

- *Circuit optimization*: Due to the area limitation, power consumption requirement and different operating conditions of high voltage devices, most conventional circuit architectures are not fit for high voltage *ASIC* design anymore. Because of large size of high voltage devices, they should be used as less as possible to decrease chip area. An efficient design methodology is to modify the existing circuit structure and divide it into a low voltage part and a high voltage part. The low voltage part can be used to achieve required functionalities in low voltage domain. And the high voltage part is used to stand with the voltage stress and boost the output voltage up to expected voltage domain. Besides the chip size, the power consumption will be greatly reduce as well while most devices are powered by low voltage power supply. Furthermore, maximum operating conditions of high voltage devices have to be take into account as well. As an example, *HVPMOS120* in *AMS H35* can stand with $120\ V$ lateral voltage (V_{DS}), but the maximum gate-source voltage of this transistor is only $20\ V$. Therefore, extra circuits are required to protect the devices in high voltage *ASIC* design.

- *Creating modules*: After selecting the circuit architecture and dividing it into different voltage domains, circuit modules should be created by using primitive elements, standard cells or module generators. Full custom design is the most flexible design but also the most difficult and costly methodology. Since many conventional circuit architectures are not suitable for high voltage applications, some circuit blocks have to be developed from scratch. To reduce the design duration and the cost, a developed set of predefined libraries is provided by the vendor. Normally, these library cells already have been fabricated and experimentally tested. Thus, the cost and risk of our own designs will be greatly reduced by using some predefined library cells.

- *Layout strategies*: In standard low voltage *ASIC* design, digital blocks and analog blocks should be separated to prevent them from coupling. Noise of digital circuits can be transported into analog circuits by substrate coupling [SVR+94], signal coupling between analog and digital signal nets [KA89], analog switch coupling [VP88], and power supply coupling. The noise isolation can be greatly increased while separating digital and analog blocks. In this way, digital and analog nets don't need to be routed near to each other except interface nets. And the separated power nets increase the substrate resistance between the analog and digital power supplies. To reduce the interference, it's also quite important to route the nets with different sensitivities separately and to avoid the coupling capacitors. Besides these conventional methodologies, high voltage *ASIC* layout has some extra challenges. The noise caused by high voltage circuit could result in a fatal error of low voltage part on chip. For example, if 1% voltage ripple of $100\,V$ power supply is transferred to $5\,V$ low voltage circuits, it will have a non negligible impact on its performances, even damage low voltage devices or cause a logic failure in digital circuits. Thus, the circuits in different voltage domains should be placed separately as well. Guard ring is required for each high voltage device to reduce this kind of influence on neighbor devices. It could lead to better circuit performances by reducing noise transfer, leakage current and latch up. However, it also consumes more chip area. To save area and power consumption, many high voltage circuit blocks also contain low voltage devices. In this case, these devices must be placed in a cluster to avoid complicated routing.

- *ERC and DRC* : Design Rule Checking is normally carried out by automatic tools to determine whether the physical layout satisfies the Design Rules provided by semiconductor manufacturers. Electrical Rule Checking is used to check the properties of a circuit which can be determined from the geometry and connectivity with understanding the behavior such as short circuits and bad connection. In high voltage circuit design, more restricted rules are used to improve circuit performance and yield. For example, the minimum active to active, well to well and metal to metal spacing have to be extended to reduce the interference between different blocks and to protect the circuit. Therefore, *ERC* and *DRC* warning reports should be clear before running post simulation.

- *Circuit simulation*: Circuit simulation is used to prove that a designed *ASIC* will work as intended. To verify the functionalities, schematic simulation and post simulation need to be done before and after layout. In a mixed signal design, entire system simulation should be carried out after verifying the digital part and the analog part separately. In order to test the digital part independently, the interface points should be designed as controllable and observable nodes from the digital part. In this way, the ability to test sub circuits separately can help locating the coming faults during verification. Furthermore, precision simulation under extreme conditions is also necessary to guarantee the circuit functionalities, especially for the analog part. The performance has to be verified at temperature, power supply voltage and process variations. Fortunately, the best and worst device models of are available and given by foundries. Thus, corner analysis even Monte Carlo simulation can be easily carried out with these models. Because of the undesired parasitics, circuit's performance can be degraded compared with the pre-layout simulation results [Tu12]. In this case, the devices' parameters, even the circuit structure have to be modified until the specification is met.

2.4 Summary

In this chapter, *CMOS* high voltage technologies have been briefly introduced in section 2.1. Several special physical structures of high voltage devices are described in details. Considering the characteristics of devices, the scaling and the desired functionalities of the circuit, *AMS H35* has been selected to implement our design. Thus, the physical structure with isolation layers of the available high voltage devices in this technology is introduced to explain the worse characteristics such as latch up and leakage current compared to devices in low voltage technologies. In section 2.2, several available high voltage digital to analog converters for different applications are presented. Based on a further discussion about advantages and disadvantages of these designs using various typologies and processes, requirements and challenges of the topic are analyzed. At last, the most important steps in high voltage *ASIC* design flow are introduced, and the main differences from the standard low voltage design are pointed out and described in details. The *ASICs* proposed in next chapters are designed following the design flow.

Chapter 3

First ASIC: An Integrated High Voltage DAC with Single Output

Contents

3.1 System Overview

The proposed high voltage *ASIC* ("Aries") design in this chapter is mainly based on our own publications [NSGRH14, NH13]. As introduced in chapter 1, in mobile and satellite communication systems, modern devices with reconfigurable antenna(*RA*) arrays are useful to operate in different frequency bands and support large number of standards(e.g., *UMTS, Bluetooth, WLAN, WiMAX*). Normally, this multi-band capability is realized by using different modules in *RF Front-end* of a device. In this way, an increment of hardware is unavoidable. To cope with this hardware increase, a better solution is to use reconfigurable microwave components to achieve multi-band capability [MSJ11] [GZM$^+$08] [MSZJ10]. This can be realized e.g. by applying semiconductor, micro-electromechanical systems and functional materials as barium-strontium-titanate (*BST*) and liquid crystal. This kind of components change their characteristics to offer multi-band functionality with the same *RF Front-end* and to compensate emerging mismatch under changing conditions. Comparing with other solutions, functional materials have higher tuning speed, smaller size, higher reliability and lower power consumption. Thus, it becomes one of the most attractive technologies to build tunable components. This kind of materials such as liquid crystal have voltage dependent capacitance and require DC or pulsed AC voltages beyond $100V$. Therefore, a high voltage digital-to-analog converter (*DAC*) which can be integrated into the system can significantly reduce the cost and the size of portable devices with such a *RF-Frontend*.

For this purpose a low voltage segmented transistor-only DAC and a linear high voltage amplifier are used to build this high voltage *DAC*. The block diagram of the system is shown in Fig. 3.1.

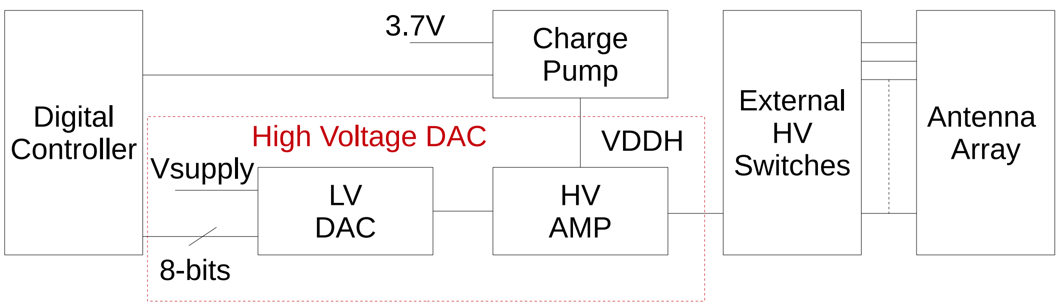


Fig. 3.1: The block diagram of the system

There are four main parts in this system. The high voltage *DAC* is powered by a nominal power supply and a charge pump which can generate high voltage up to $120\ V$ from a battery with $3.7\ V$. A micro controller is used to generate four phase clock for the charge pump and the input code for the high voltage *DAC*. With an external high voltage switches it can provide individual voltages for each channel in antenna arrays.

3.2 Design Implementation

Considering the cost, the size and the accuracy of the high voltage *DAC*, the proposed *HV ASIC* design is divided into two individual parts, a low voltage *DAC* and a high voltage amplifier. Comparing with a single high voltage *DAC*, this structure consumes smaller current from the high voltage power supply and has more accurate output.

3.2.1 Low Voltage DAC

Data converters are very basic and important circuit blocks in most modern communication systems. In a system, operations like filter, decimation, addition, subtraction and other mathematical operations can be easily performed on digital signals using a digital signal processor. Thus, natural signals in real world are required to be converted to digital signals by using a analog to digital converter. However the digital signal coming from *DSP* could not be used as the output voltage. Normally, the output voltage level of the system is relevant to specific purposes. Therefore, a digital to analog converter is required to convert the digital data back to analog domain. In this thesis, a *DAC* is used to convert the digital signals to the analog outputs with 256 voltage steps to fulfill the requirement of the functional materials used to build reconfigurable microwave devices.

The input signal of a *DAC* should include a digitally coded and quantized input and a reference clock signal. According to specific applications, the digital input is converted to an analog entity like voltage, current or power. The most important specifications needed to be considered and measured are following:

- *Resolution*: It is the smallest amount of variance in output voltage as a fraction or percentage of the full-scale output voltage range for the different digital input.
- *Monotonicity*: A *DAC* is defined to be non-monotonic if its output voltage decreases with an increase in the digital input. The output voltage of a monotonic *DAC* increases regularly while its binary digital input increasing form one code to the next.
- *INL*: Integral non linearity is a static linearity specification referred to as relative accuracy. It expresses the deviation of the actual output voltage from the ideal as offset and gain error being calibrated out of the measurement. Since it describes the precision of its output voltage, it is usually considered to be the most valuable specification to evaluate if the performance could fulfill the precision requirement of the applications.
- *DNL*: Differential non linearity expresses the voltage difference between two adjacent digital input codes from the ideal voltage step ($1\ LSB$). It is related to the *DAC* monotonicity and to be used to determine if the *DAC* has any missing code.
- *Offset Error*: Offset error is a constant voltage difference between the actual and the ideal finite resolution characteristic measured at any vertical jump.
- *Gain Error*: Gain error is the difference in slop of the actual output voltage curve and the ideal output voltage curve. Since the second chip presented in this dissertation has 16 outputs, each *DAC* could have different gain error. Thus, it must be considered as a very important specification in this design.

- *Settling time*: Any change in the digital input will not be reflect in the analog output voltage immediately. The time required for the output voltage to settle to the voltage within $(1/2)\ LSB$ of the expected value is defined as settling time.

Many methods exit to design high speed and high accuracy *DACs* for different applications. The advantages, disadvantages and specifications are discussed to select a proper topology to implement the low voltage part in the proposed design.

- *R String DAC*: It is the simplest *DAC* structure. An N-bits version of *R string DAC* consists of 2^N resistors of the same value in series and 2^N switches built in CMOS transistors. Each switch is connected between one node of the resistor chain and the output. It is inherently monotonic and compatible with purely digital technologies, but this topology is only suitable for designing *DACs* which require resolution higher than 8-bits and high settling time.

- *R2R DAC*: Another popular *DAC* structure is *R2R ladder network*. Only two resistors' sizes are used in this architecture. Because of the ratio of these transistors is $2:1$, this structure is called *R2R DAC*. With this topology, an N-bits *DAC* requires 2N resistors which are easily trimmed. *R2R ladde*r can be used as the voltage mode and the current mode, which are called "normal" mode and "inverted" mode, respectively. Compared to *R string DAC*, this topology consumes less area and much easier to be implemented. But the resolution is also quite limited.

- *Switched capacitor DAC*: *Binary-weighted DAC* structure can also be implemented using capacitors to scale charge and divide capacitive voltage. This topology requires large area of capacitors for high *DAC* resolution. For example, the area of *MSB* capacitor is 512 times larger than the *LSB* capacitor for a 10-bits *DAC*. The most important advantages are low power consumption and the possibility to be calibrated. This structure has low power consumption because the capacitor array doesn't dissipate any DC power, and calibration technique and offset cancellation methods can be easily implemented for improving performance. On the other side, the monotonicity depends on the element matching, and the leakage could cause it to lose its accuracy after being set. Therefore, an appropriate technology having good capacitive material is required to ensure the accuracy.

- *Current steering DAC*: Switched current sources in *Current Steering DAC* are built in *CMOS* transistors instead of resistors to provide higher operation speed. *Binary-weighted Current Steering DAC* consists of N unit cell for N-bits *DAC*. The biggest problem with this topology is mismatch of the transistors. *W2W* structure consists of the transistors of only two size(W/L and $2W/L$) and solves the mismatch problem. *Current Steering DAC* could operate very fast and achieve relatively high resolution around 10-bits by selecting a reasonable length of the transistors. The most important disadvantage is the technology dependent accuracy. The device size (W/L) and the variation of Vth have significant impact on the specifications.

- *Transistor only R2R DAC*: Be different from *Current Steering DAC*, transistors in this topology has the same W/L ratio and are working in linear region. All transistors including those used as switches are working in deep linear region and viewed as resistors. Since the source to drain voltage should be set to a relatively small value to ensure that the transistors are working in linear region, the power consumption is much less compared to *Current Steering DAC*. The *INL*, *DNL* and gain error are also strongly dependent on process and mismatch variations of the selected technology.

- *Oversampling DAC*: *Oversampling DAC* such as *Delta-sigma DAC* is another popular topology to implement the data conversion function for applications requiring medium-to-low speed and high resolution. Oversampling means sampling the input data at a frequency greater than the Nyquist frequency, and the quantization noise in the low frequency band are greatly decreased. Normally, it consists of a *Delta-sigma Modulator* implemented with digital technology to produce the bitstream and an analog low pass filter. A *Delta-sigma DAC* first encodes a high resolution digital input data into a low resolution signal by sampling the signal with a relatively higher sampling frequency. The sampled low frequency signal is mapped to voltages and can be smoothed with an analog low pass filter. To evaluate performances of *Oversampling DACs*, not only time domain specifications but also frequency domain specifications have to be measured. The most important specifications are signal-to-noise ratio (*SNR*), spurious free dynamic range(*SFDR*), distortion and settling time. A primary advantage of *Oversampling DAC* is the relaxation of the requirements on the analog part: reduced matching tolerances, relaxed anti-aliasing specs and relaxed smoothing filters. It could achieve high resolution in relatively low speed as consuming more power and larger area.

For antenna arrays which are applied by using functional materials, few kilo Hertz can fulfill their speed requirement. Therefore, the frequency requirement is not the key feature in this design. According to the application, the proposed *ASIC* should be able to be integrated into hand-held devices powered by battery. Thus, the power consumption becomes the biggest challenge. To decrease the hardware size and complexity, the chip area should also be one of the most important specifications.

Based on the requirements of the application, the minimum voltage step should not be larger than $0.5\ V$. The voltage range is from $0\ V$ to $115\ V$ that can be fulfilled with 8-bits *DAC*. Although most introduced topologies can meet the resolution requirement, *Transistor Only R2R DAC* and *Current Steering DAC* consume relatively low power and much easier to be implemented than *DACs* built in resistors. Both are very suitable for our application. Compared to *Current Steering DAC*, voltage mode *Transistor Only R2R DAC* requires more reference voltages and a negative power supply but consumes less power. In the first design, *Transistor Only R2R* topology is chosen to implement the low voltage *DAC*. In the second design, to eliminate the negative power supply and reach the maximum high voltage range($0\ V$ to $120\ V$), current steering topology is used to implement the data conversion functionality.

3.2.1.1 Segmented Transistor-Only DAC

Compared with other devices, *CMOS* transistors can work with a relatively low current of a few micro ampere. Thus, it is feasible to design a transistor only *DAC* to reduce the power consumption and increase the integration density of the chip. Fig. 3.2 shows the structure of the 8-bits low voltage *DAC*. In this *DAC*, instead of resistors or capacitors, transistors working in linear region used for accurate voltage division will consume less power than working in saturation region.

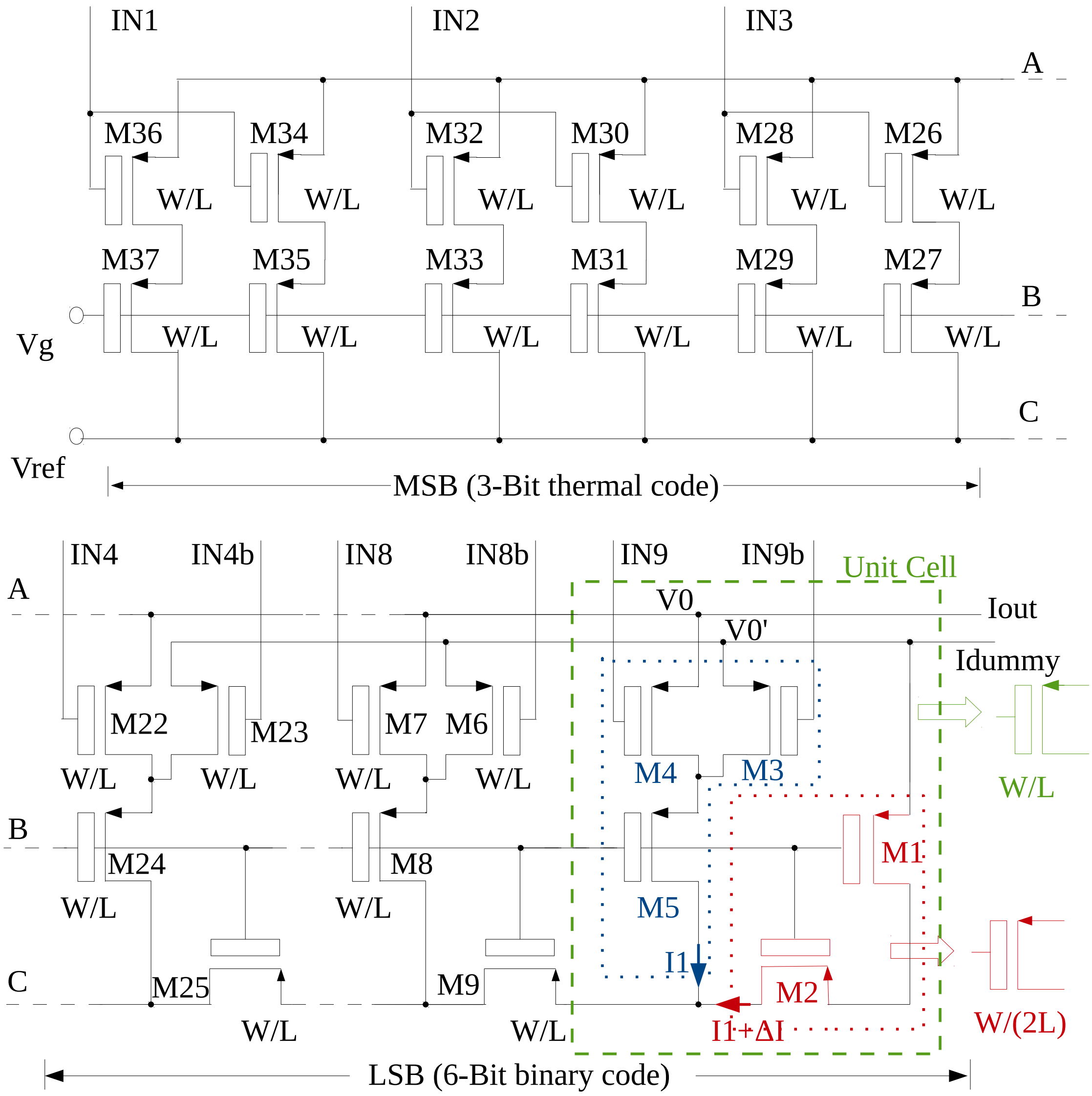


Fig. 3.2: 8-bits low voltage transistor-only DAC

Although transistor only R2R topology can achieve 8-bits resolution, the worse characteristics of devices in this high voltage technology could lead to unexpected lose in performance of the *DAC*. The significant error is the current mismatch of the two branches in each unit cell as shown in Fig. 3.2. Therefore, a few binary bits should be replaced with unary ones. To achieve good linearity and avoid high glitch energy, this *DAC* is divided into two sub-DACs. The least significant bits are binary coded, and the most significant bits steer a unary current array. The two most significant bits are converted to 3-bits thermal code which is used to control the unary current array as showed in Fig. 3.3. The flip-flops in the circuit are used to synchronize the output signals. The pre-layout simulation result of the binary to thermal code decoder is shown in Fig. 3.4. The output signals of the decoder are used to switch the *MSB* part on/off in the *DAC*. This *MSB* part can be viewed as an equivalent circuit in Fig. 3.5. Since all transistors are working in linear region, they can be viewed as resistors in this equivalent circuit. Each bit of the thermal code controls two branches to generate current. Thus, two branches are switched on when in2 is low, and four branches are switched on as in1 is low.

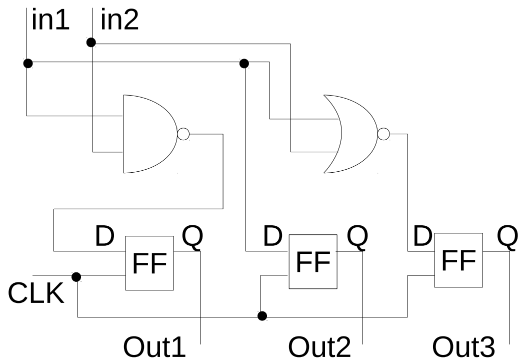


Fig. 3.3: Schematic of the binary to thermal code decoder.

A unit cell in the binary array is shown in the dashed rectangle in Fig. 3.2. All transistors have the same aspect ratio (W/L). Transistors $M1$, $M2$ and $M5$ have the same gate voltage V_g, and the transistors $M3$ and $M4$ are controlled to be switched on/off by one bit digital signal, whose voltage is shifted to the same voltage level as V_g. Transistors in series ($M1$ and $M2$, $M3$ (or $M4$) and $M5$) can be viewed as an equivalent transistor with an aspect ratio equals to $W/(2L)$. The unit cell is composed of two equivalent transistors in parallel and can be viewed as one composite transistor with an aspect ratio equals to W/L. Unlike traditional current steering digital to analog converters, all transistors in this *DAC* are biased in linear region. Therefore, the *LSB* (the least significant bits) part can be viewed as an *R2R DAC* as shown in Fig. 3.6, which is composed of transistors in series and in parallel. If the LSB current in this DAC is I, other current units will generate a current of $2^N I$. N is the bit number. Thus, the output current range of the DAC will be from 0 to $256I$.

Choosing a small drain-source voltage($V_{ds} \ll V_{gs} - V_{th}$) will make the transistors working in deep linear region and greatly reduce the second-order effect(V_{th} variation). Furthermore, the mismatch caused by threshold voltage variation can be reduced by choosing a large overdrive voltage ($V_{gs} - V_{th}$). In this paper, $V_{gs}(V_g - V_0)$ is $2.5V$, V_{th} is $1.0V$ [Tec60]

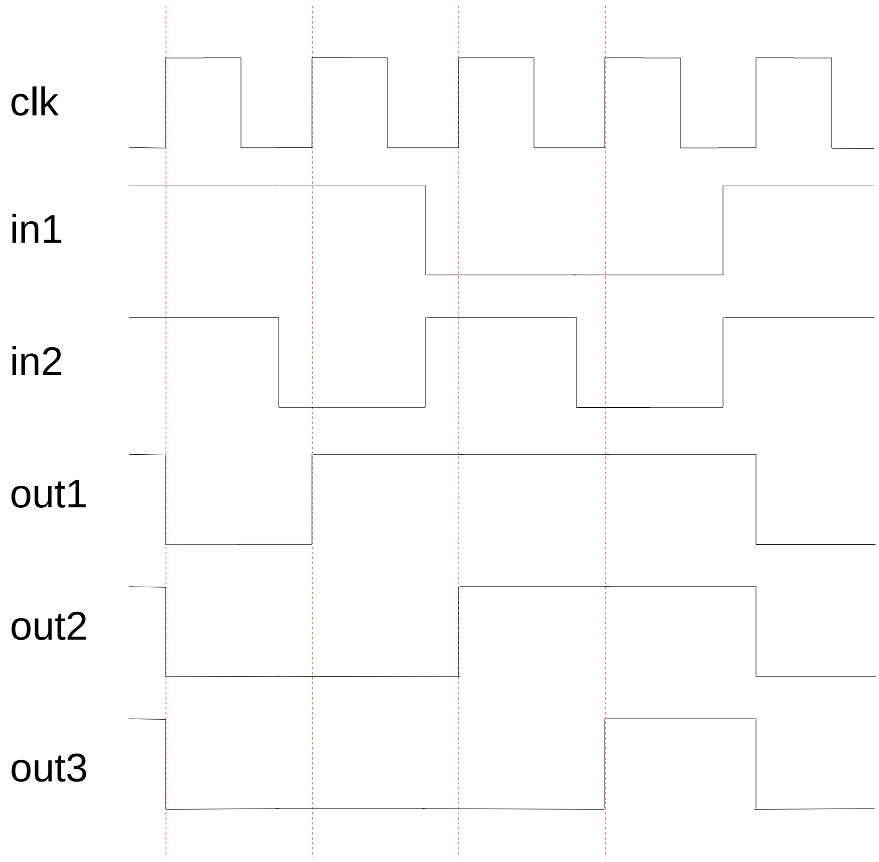


Fig. 3.4: Pre-layout simulation result of the binary to thermal code decoder.

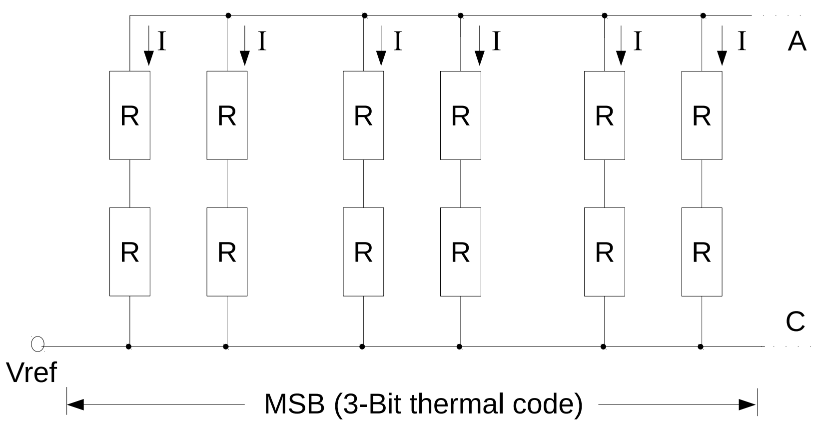


Fig. 3.5: Equivalent circuit of the MSB part in the 8-bits DAC.

and $V_{ds}(V_{ref} - V_0(\text{ or } V_{0'}))$ is $250\,mV$. The reference voltage generator will be presented in section 3.2.1.

To choose the proper size of the transistors, two most important specifications must be taken into account. One is Integral Non Linearity(INL) which expresses the deviation of the actual output voltage from the ideal as offset and describes the precision of its output

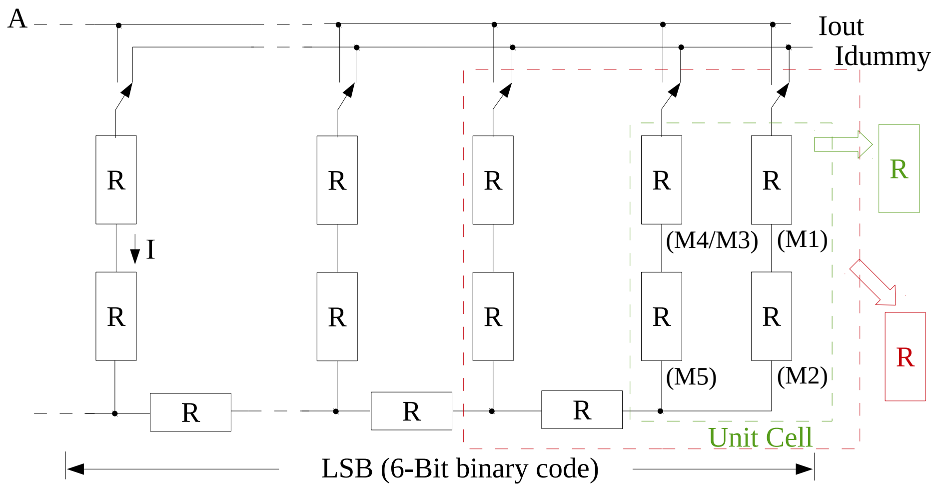


Fig. 3.6: Equivalent circuit of the LSB part in the 8-bits DAC.

voltage. The other one is Differential Non Linearity (DNL) which is related to the DAC monotonicity and expresses the voltage difference between two adjacent digital input codes from the ideal voltage step (1 LSB). Based on the mismatching properties of MOS transistors [PDW+89], *INL* and *DNL* estimates are given by the following equations.

$$INL = \sqrt{2^{(N-2)}}\frac{\sigma I}{I} \tag{3.1}$$

$$DNL = \sqrt{2^{(N'+1)} - 1}\frac{\sigma I}{I}LSB \tag{3.2}$$

N is the number of bits, and N' is the number of unary unit cells. According to the voltage dependent electronic magnetic property of the functional materials, the deviation of the biasing voltage applied in tunable devices must be less than $0.5\ mV$ to ensure that the reconfigurable microwave components can change their capacitance properly. The output voltage of this low voltage DAC will be boosted up by a high voltage amplifier which will be proposed in section 3.2.2. The voltage step of the high voltage output is $0.45\ V$. To fulfill the accuracy requirement of the biasing voltage applied in tunable devices, both INL and DNL should be less than one LSB. From the results given by the reference [VdBSS01], the minimum WL area can be calculated by using the following equation:

$$(WL)_{min} = \frac{[A_\beta^2 + \frac{A_{vto}^2}{(Vgs-Vth-\frac{1}{2}Vds)^2}]}{(\frac{\sigma I}{I})^2} \tag{3.3}$$

A_β^2 and A_{vto}^2 are transistors' matching parameters, and σI is the current variation. $\frac{\sigma I}{I}$ depends on the required *INL* yield. By using *INL* yield equals to 99.7%, the minimum gate area (WL) is $36.5\mu m^2$ ($W/L = 8\mu m/5\mu m$). The maximum output current of this 8-bits *DAC* is $49.78\mu A$, and the *LSB* current is $0.21\mu A$. Therefore, maximum power consumption of the current mode *DAC* is $0.013\ mW$. Since the output voltage has to be boosted up by using a *HV* amplifier, the output of the current mode *DAC* required to be converted to voltage mode with a low voltage amplifier as shown in Fig. 3.7.

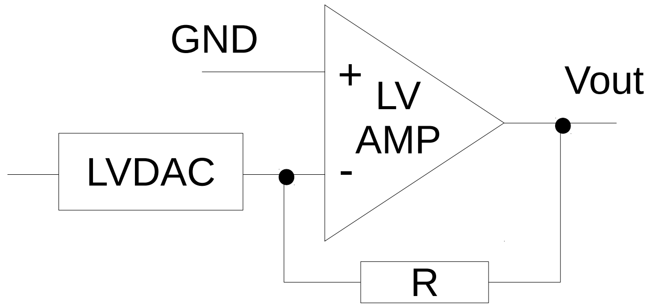


Fig. 3.7: Voltage mode low voltage DAC.

Based on the pre-layout simulation result, the performance of the low voltage digital to analog converter is calculated. The ideal output range and voltage step are 0-$2.5\,V$ and $0.01\,V$, respectively. The output range of simulation result is $0.40\,mV$-$2.498\,V$. The offset error and gain error are $0.40\,mV$ and $0.19\,LSB$, respectively. The maximum *INL* of the DAC is $0.31\,LSB$, and the maximum *DNL* of the DAC is $0.27\,LSB$ as shown in Fig. 3.8 and Fig. 3.9.

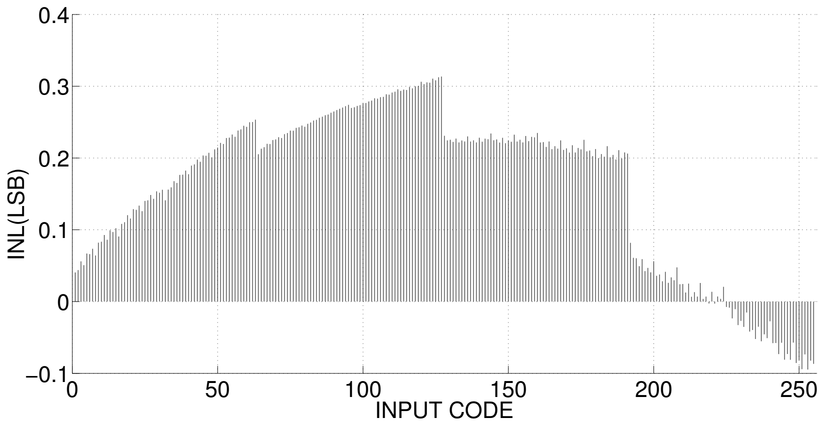


Fig. 3.8: INL of the low voltage DAC in pre-layout simulation.

3.2.1.2 Reference Voltage Generator

The output current of the *DAC* is converted to voltage by using an operational amplifier with resistive feedback ($R1$) given in Fig. 3.10. As shown in Fig.3.2, the *MSB* part can be viewed as three transistors with an aspect ratio equals to W/L in parallel, and the *LSB* part can be viewed as one transistor with the same W/L ratio. The full scale output current of the low voltage *DAC* depends on V_{th}, V_{ref} and V_g of these four parallel transistors. Therefore, the variations of V_{th} and V_{ref} are the major factors contributing to gain error as

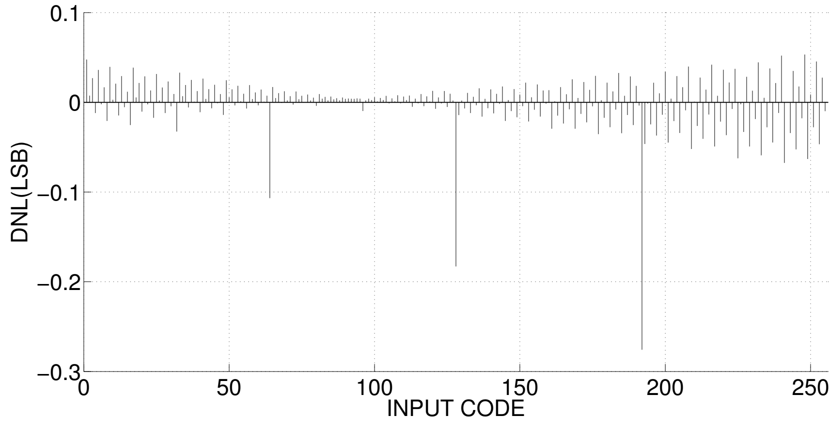


Fig. 3.9: DNL of the low voltage DAC in pre-layout simulation.

the transistors having fixed gate voltage (V_g). The reference voltage generator given in Fig .3.10 generates V_{th} dependent reference voltage (V_{ref}) to decrease the gain error caused by process variations.

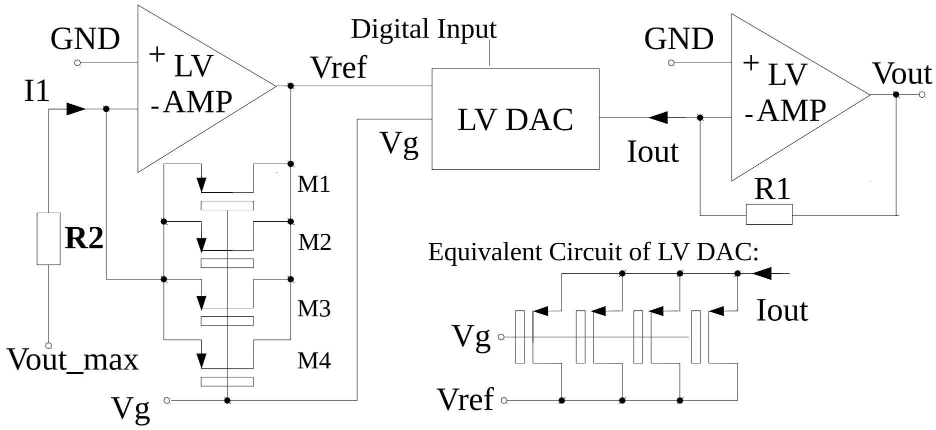


Fig. 3.10: Reference voltage generator

When V_{out_max} is set to the required full scale voltage of the *DAC*, and the two resistors ($R1$ and $R2$) have the same resistance value, the voltage generator will generate a desired V_{th} dependent reference voltage (V_{ref}). As shown in this figure, the four parallel transistor($M1$ to $M4$) and the equivalent circuit of the low voltage *DAC* have the same V_S, $V_{ref}(V_D)$ and V_g. Therefore, the full scale output current (I_{out}) equals to $I1$ and guarantees a fixed output voltage range (0 to V_{out_max}). Thus, this structure reduces the gain error caused by various V_{th} during fabrication.

3.2.2 High Voltage Amplifier

The digital input signal is only used in low voltage part of this circuit. To achieve required high voltage up to $115\ V$, the output of the *DAC* has to be boosted up by a high voltage amplifier. The structure is given in Fig. 3.11.

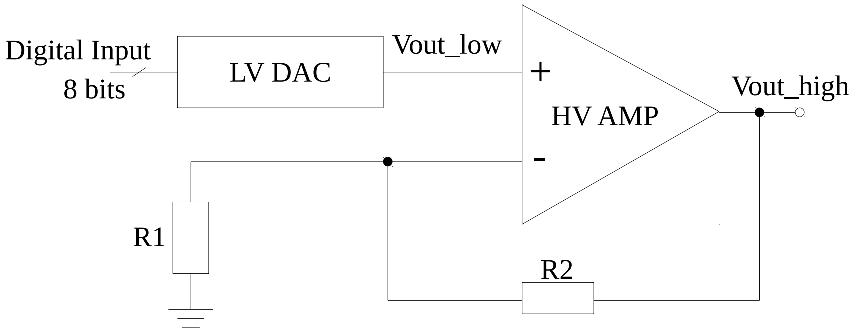


Fig. 3.11: The structure of the high voltage digital-to-analog converter

Many different amplifier topologies are available for different applications. The most conventional two architectures are folded cascode amplifier and two stage miller compensated amplifier. Compared to two stage miller compensated amplifier, folded cascode topology has a higher gain bandwidth for the same current, a higher output impedance and a larger input common mode range. Besides, it is much easier to be stabilized as the second pole is much greater in magnitude than in two stage opamp. The disadvantages of folded cascade topology are limited output swing, higher power consumption and higher noise.

In this design, since the high voltage devices occupy most chip area, reducing the number of the high voltage devices becomes the most primary task. In folded cascode amplifier, more transistors are required in output stage. These transistors have to be able to stand with high voltage up to $120\ V$, which means they should be implemented by using *HV* devices. Due to the large size of the high voltage transistors, this topology will consume more area than two stage miller compensated amplifiers. Since this design is expected to be used in mobile devices, the power consumption also becomes a very important specification. In folded cascode topology, the output stage contains two branches, whose bias current are the same, to convert the differential output to a single output. Therefore, the required bias current from $120\,V$ power supply is twice larger than in two stage amplifier. Considering the area and power consumption, two stage miller compensated topology has been selected to implement the *HV* amplifier.

3.2.2.1 High Voltage Amplifier Architecture

The *HV* amplifier is implemented using a two stage miller-compensated operational amplifier based on the proposed structure for applications up to $27\,V$ [ASH06]. In *AMS H35*, the drift region of *HV* transistors can be considered as two parts, the low voltage part and the high voltage part as shown in Fig. 3.12. The extra high voltage drift region is the reason that high voltage transistors can stand with a very high lateral voltage. With isolation layers and extended regions on drain, the maximum operation voltage of these transistors can reach up to $120\,V$ ($V_{DS\_MAX} = 120V$). There are three gate oxidation layers available in the technology. The gate-source voltage can reach $20\,V$ by using the thickest oxidation layer ($V_{GS\_MAX} = 20V$). Because of the special physical structure, these high voltage transistors have relative larger size than low voltage devices. Fortunately, both standard low voltage devices and high voltage devices are available in this technology, and they can be easily integrated into one chip to greatly reduce the chip size. Thus, the *HV* transistors are only used in the second stage to block high voltages. As shown in Fig.3.13, the first stage is designed using *LV* transistors and the second stage has six *HV* transistors.

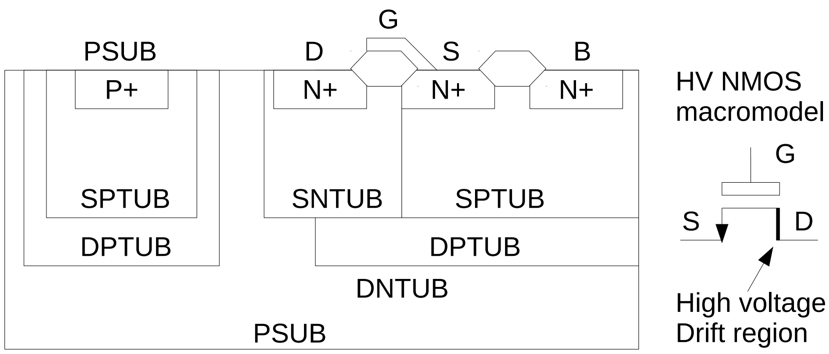


Fig. 3.12: The structure of HV NMOS transistor in AMS H35

The cascade *HV* voltage transistors ($M2$, $M3$, $M6$ and $M7$) in the second stage are used to block high voltage. The *LV NMOS* transistors ($M8$ and $M16$) compose a current mirror to provide static current for the second stage. The current mirror consists of *LV* transistors is more accurate than that built in *HV* transistors. Since the maximum voltage between drain and p-substrate of *LV* transistors is limited to $50V$, another current mirror composed of $M1$ and $M5$ can not be replaced by *LV* current mirror. Four *LV* transistors($M17$, $M18$, $M19$ and $M20$) are used as diodes to protect the drain source voltage of $M14$ exceeding the safe operation area($5\,V$).

In this op amplifier, the first stage consumes current of $25\,\mu A$ from *LV* power supply, and the bias current of $M5$ is $8\,\mu A$. The static current of the output stage depends on W/L ratios of $M1$ and $M5$. To achieve a relative higher slew rate, $(W/L)_1$ has to be much larger than $(W/L)_5$. In this circuit, the current of the output stage is $70.7\,\mu A$ while $(W/L)_1$ equals to $9*(W/L)_5$. Since the total current draws from *HV* supply is less than $100\,\mu A$, the *HV* amplifier can be powered by a nominal low voltage power supply and a high voltage supply generated by a charge pump. The power consumption of the *HV* amplifier is only $9.07\,mW$.

In this structure, the feed-back loop ($R1$ and $R2$) shown in Fig. 3.11 consumes current from the high voltage supply as well. To reduce the impact on the slew rate of the output stage, the resistors must be sufficiently large to decrease the current consumption. The

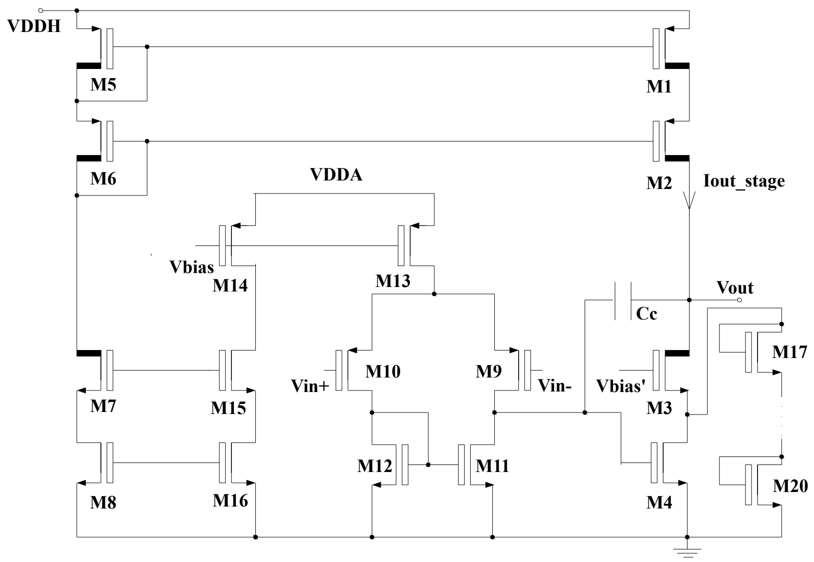


Fig. 3.13: The structure of the high voltage amplifier

high voltage output of the *HV DAC* can be calculated by the following equation:

$$V_{out} = \frac{(R1 + R2)}{R1} V_{out\_low} \tag{3.4}$$

In this circuit, $R1$ equals to $0.1M\Omega$, and $R2$ equals to $4.5M\Omega$. With the full-scale voltage ($115\ V$), the maximum static current consumption of these feed-back resistors is $25\ \mu A$.

3.2.2.2 Pre-layout Simulation of High Voltage DAC

In our application, this high voltage *DAC* is considered to drive 64 individual channels of antenna arrays. Thus, 64 switches have to be used for the interface. The external commercial switches have off capacitance of $12\ pF$. Besides the parasitic capacitance of switches, the input impedance of the antenna array should be taken into account to calculate the load capacitance of the high voltage amplifier as well. The input impedance of each channel is normally between $10\ pF$ and $20\ pF$. Therefore, the total load capacitance can be calculated by the following expression:

$$C_{Load} = 64 * C_{sw} + C_{antenna} \tag{3.5}$$

To estimate the settling time of the output voltage in the worst case, the simulation is carried out with a load capacitance of $800\ pF$. Fig. 3.14 shows the pre-layout simulation result of the output voltage. As shown in this figure, it takes $2.3\ ms$ to charge the load capacitor from $0V$ to $115V$. In the worst case, it will take $147.2ms$ for 64 channels reaching $115\ V$.

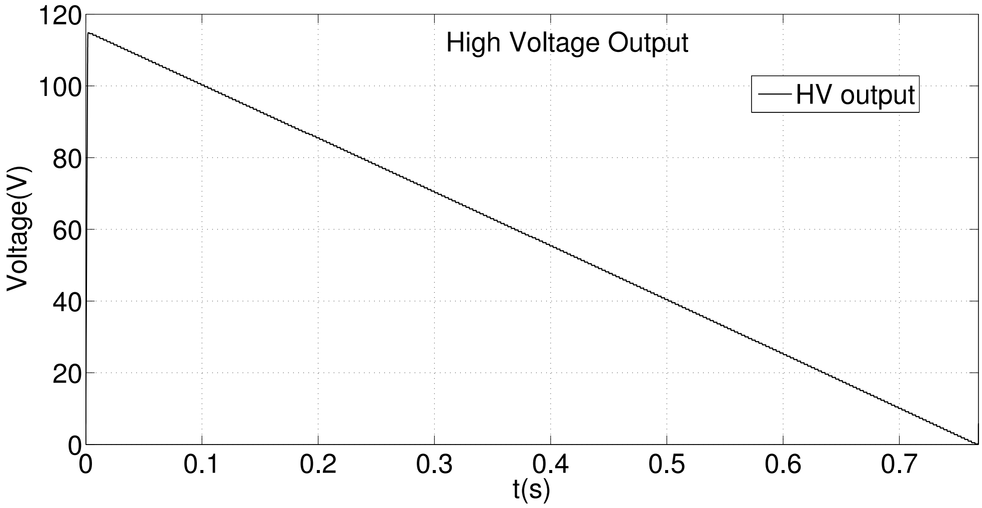


Fig. 3.14: Pre-layout simulation result of the output voltage.

The offset error and gain error are $122\ mV$ and $0.24\ LSB$, respectively. As shown in Fig. 3.15 and Fig.3.16, the maximum *INL* and *DNL* of this high voltage *DAC* are $0.32\ LSB$ and $0.28\ LSB$, respectively. Compared to the simulation result of low voltage *DAC*, the offset error, gain error, maximum *INL* and maximum *DNL* are much larger. The *INL* and *DNL* errors mainly come from the low voltage *DAC* and mismatch of the input pair in the high voltage amplifier. Then the errors will be amplified by the close loop architecture. Besides, drain-source voltage drop of $M3$ and $M4$ in the second stage of the high voltage amplifier has major impact on the offset error as well. In like manner, the highest output voltage can not reach $115\ V$. Thus, the scaling of $M1$ and $M2$ plays an important role in reducing the gain error.

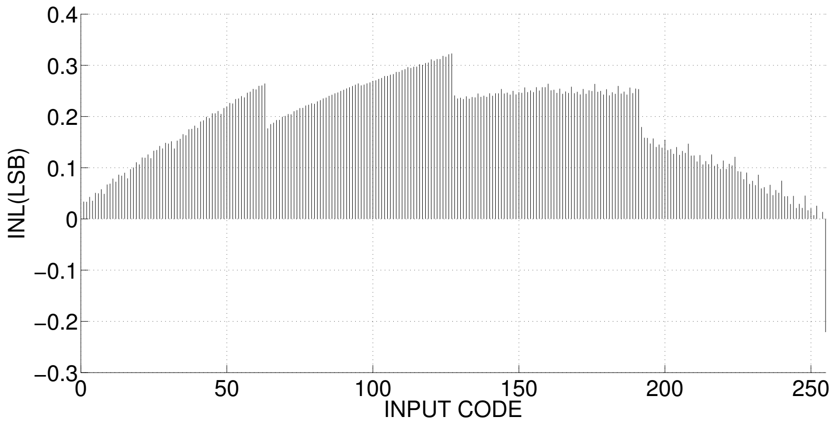


Fig. 3.15: INL of the high voltage DAC in pre-layout simulation.

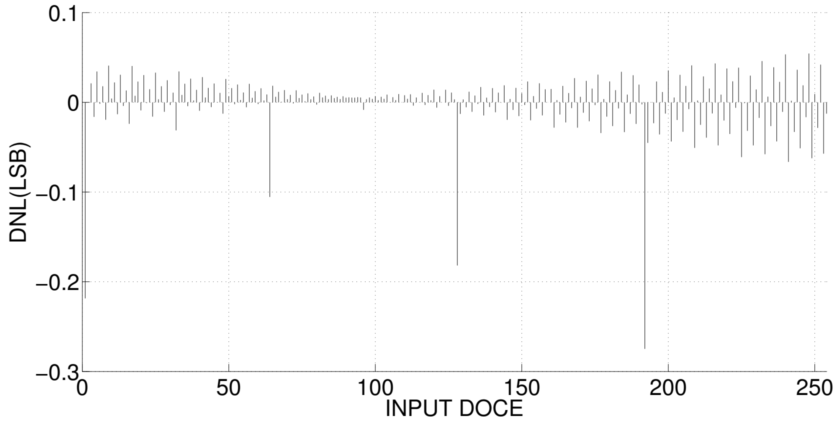


Fig. 3.16: DNL of the high voltage DAC in pre-layout simulation.

3.3 Chip Fabrication: "Aries"

Comparing with low voltage technology, the layout of high voltage SOC is more sophisticated. In general high voltage devices are larger than low voltage de- vices. Guard ring is required for each HV device to reduce leakage current and latch-up. Furthermore, the spacing between HV devices and HV metals has to be larger as well. Therefore, the chip size will be relatively large.

3.3.1 Layout of the Low Voltage DAC

Since this high voltage technology has larger parasitics than low voltage ones, it's necessary to select a proper layout strategy to reduce the functional errors caused by mismatch of devices in the circuit. As shown in Fig. 3.2, each *LSB* current unit in the architecture has four transistors with the same W/L ratio, and each *MSB* unit has two current branches consisting of four transistors as well.

To reduce the mismatch of the transistors inside of the current unit, each transistor is divided into four small devices. Thus, 16 small transistors are placed as a $4 * 4$ array and connected as shown in Fig. 3.17.

To reduce the influence of the parasitics, the lowest significant unit cell is put in the middle of the layout. The rest unit cells are placed from the middle to the margins in order as shown in Fig. 3.18.

After *DRC* and *LVS* check, post-layout simulation is carried out to verify the functionalities of the circuit. Normally, because of the parasitics the post-layout simulation result is worse than the pre-layout simulation one. Based on the post-layout simulation result as shown in Fig. 3.19 and Fig .3.20, maximum *INL* and maximum *DNL* are calculated. The maximum *INL* and *DNL* are $0.39\ LSB$ and $0.30\ LSB$, respectively. The offset error is $0.57\ mV$, and the gain error is $0.28\ LSB$.

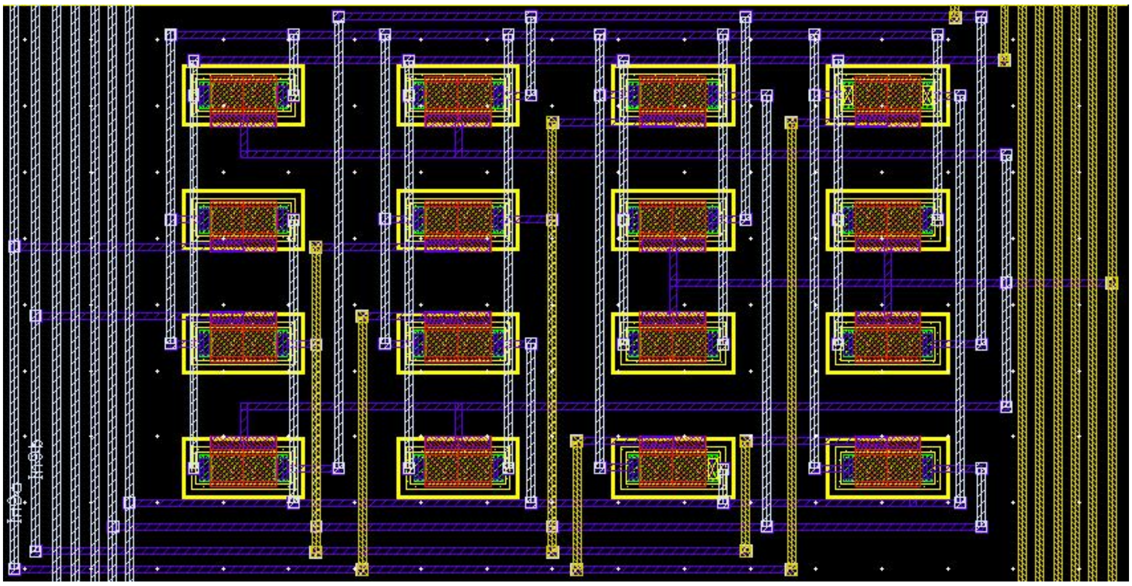


Fig. 3.17: Layout of one unit cell in the low voltage DAC.

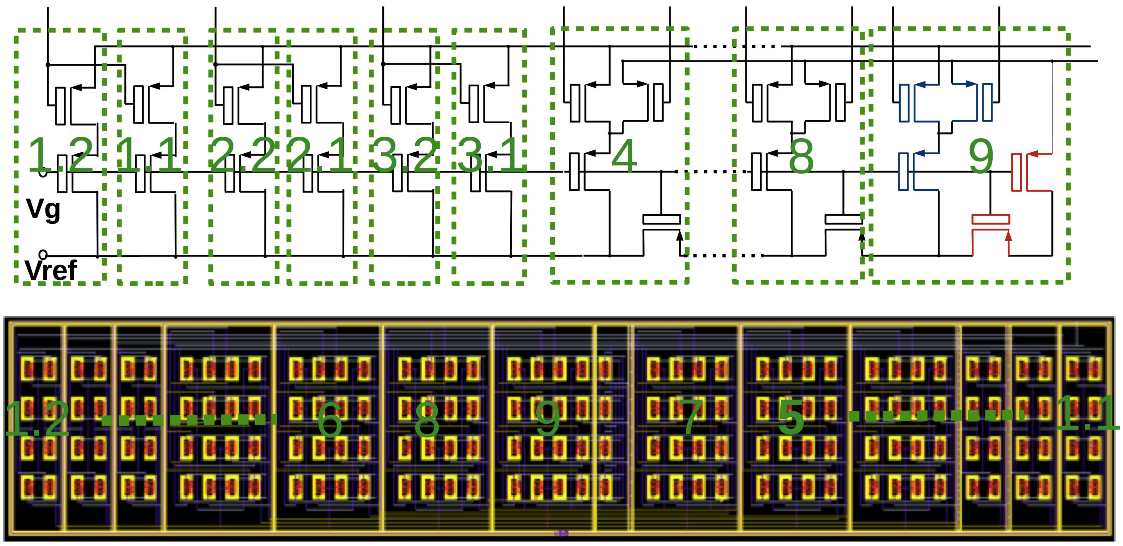


Fig. 3.18: Layout of the low voltage DAC.

3.3.2 Layout of the High Voltage Amplifier

Compared to low voltage devices, the scaling of high voltage devices is much larger. To reduce the chip size, high voltage transistors are only used in the second stage of the high voltage amplifier to stand with high voltage. As shown in Fig. 3.21, low voltage devices and high voltage devices are separated into different clusters. According to design rule of this technology, all *NTUB* should be surrounded by a guard ring to reduce the leakage current and cross talk between neighbor devices. Gathering all low voltage devices on one *NTUB* results in the possibility to share a guard ring and reduce the chip size. Because of the sophisticated physical structure, guard ring is required by each high voltage

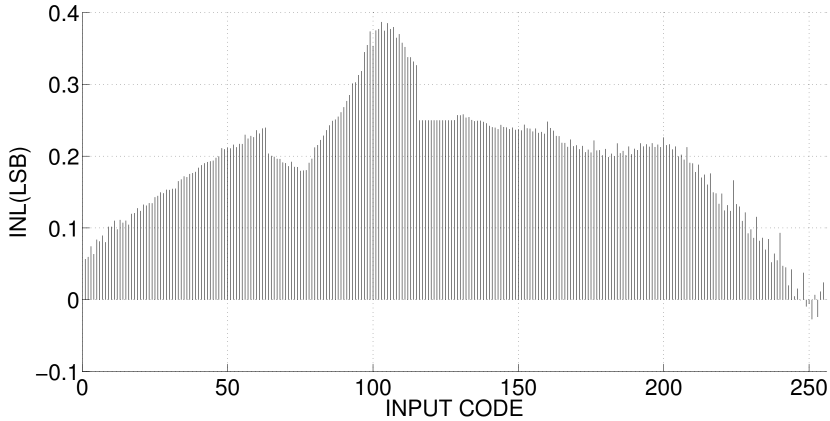


Fig. 3.19: INL of the low voltage DAC in post-layout simulation.

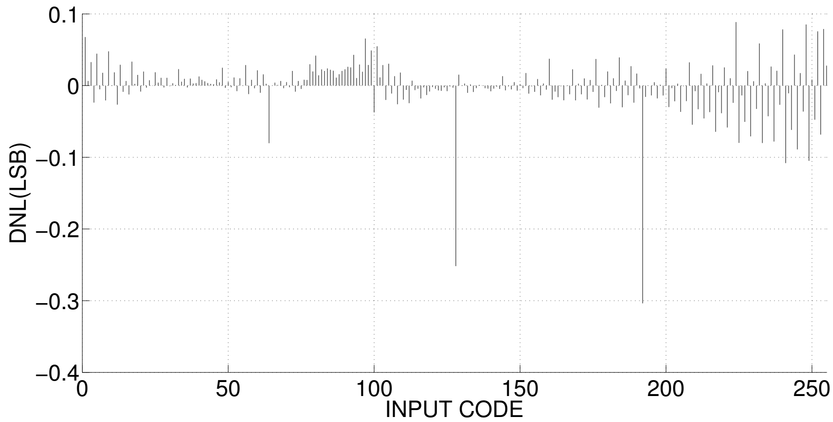


Fig. 3.20: DNL of the low voltage DAC in post-layout simulation.

transistor. In this figure, the low voltage part is put on the left side, and the high voltage transistors are arranged on the right side. Compared to the low voltage part, these six high voltage transistors are much larger and consume most chip area.

The post simulation result of this high voltage amplifier is shown in Fig. 3.22. The maximum load capacitance including off capacitances of switches is $800\ pF$. Therefore, the simulation is carried out with a load capacitance of the $800\,pF$ in Cadence. The upper curve in this figure shows the logarithm of the amplitude of the gain, and the lower curve plots the phase of the output signal of the high voltage amplifier. Both gain and phase versus frequency on logarithmic scale. The bandwidth of the amplifier is relative low with such a high load capacitance and the required miller capacitance in the amplifier. As shown in this figure, the maximum gain is $86.29\ dB$, and the bandwidth is $88\ KHz$.

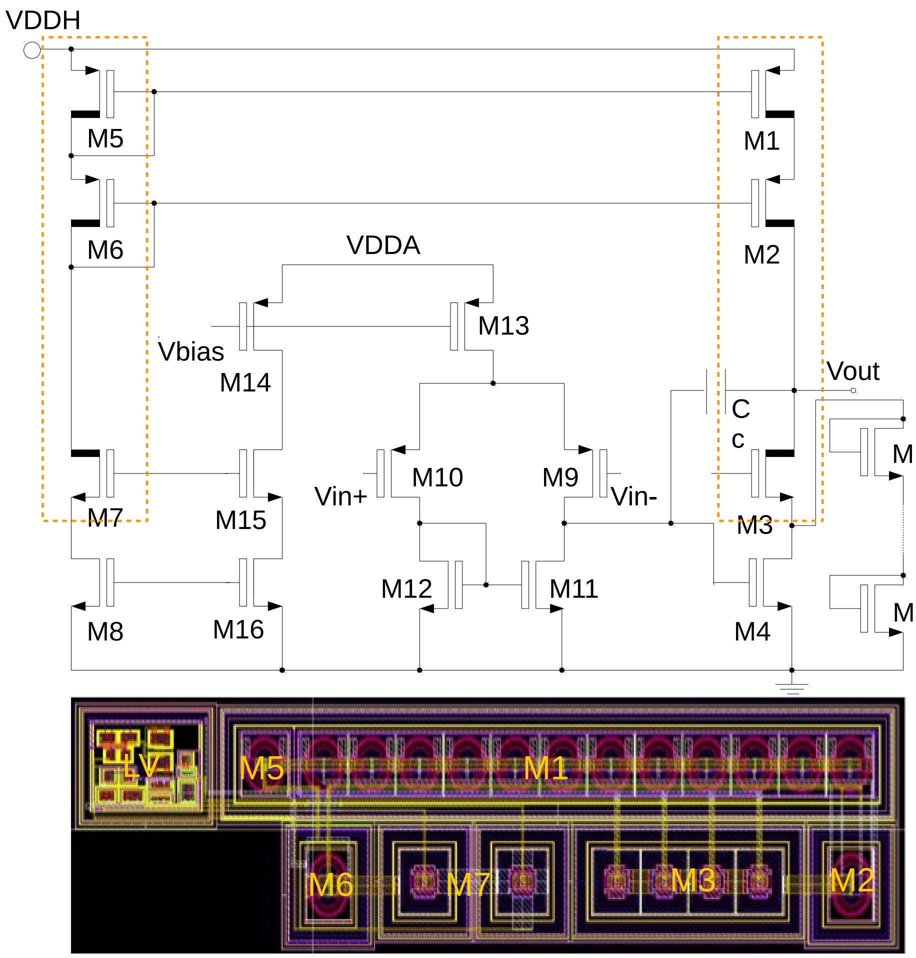


Fig. 3.21: Layout of the high voltage amplifier.

3.3.3 Post-layout Simulation of the Chip

Layout of the high voltage *DAC* is shown in Fig. 3.23. Besides the low voltage *DAC* and the high voltage amplifier, some other sub-circuits such as voltage reference, decoder and voltage regulator are also included. Due to the large size of high voltage *ESD* protection devices, high voltage pads (power pads and input/output pad) also have larger size than that of low voltage circuit. The largest on the right side in this figure is a $120\ V$ output pad. The size of this pad is $300\mu m * 360\mu m$. It obviously has a big impact on chip size. In addition, since multiple power domains exist on chip, substrate cut elements are also required to separate the power and ground signal in digital, analog and high voltage domains. Because of the huge high voltage pads, this layout is pad limited. The layout size of the entire chip including pad frame is $3.5\ mm^2$.

To verify the functionality and estimate the impact of the parasitics, post-layout simulation is carried out with the same load capacitance in the pre-layout simulation. The output result of the transient simulation is shown in Fig. 3.24. The settling time from $0\ V$ to $115\ V$ is $2.3\ ms$. Since the load capacitor is $800\ pF$, the parasitic capacitors can be

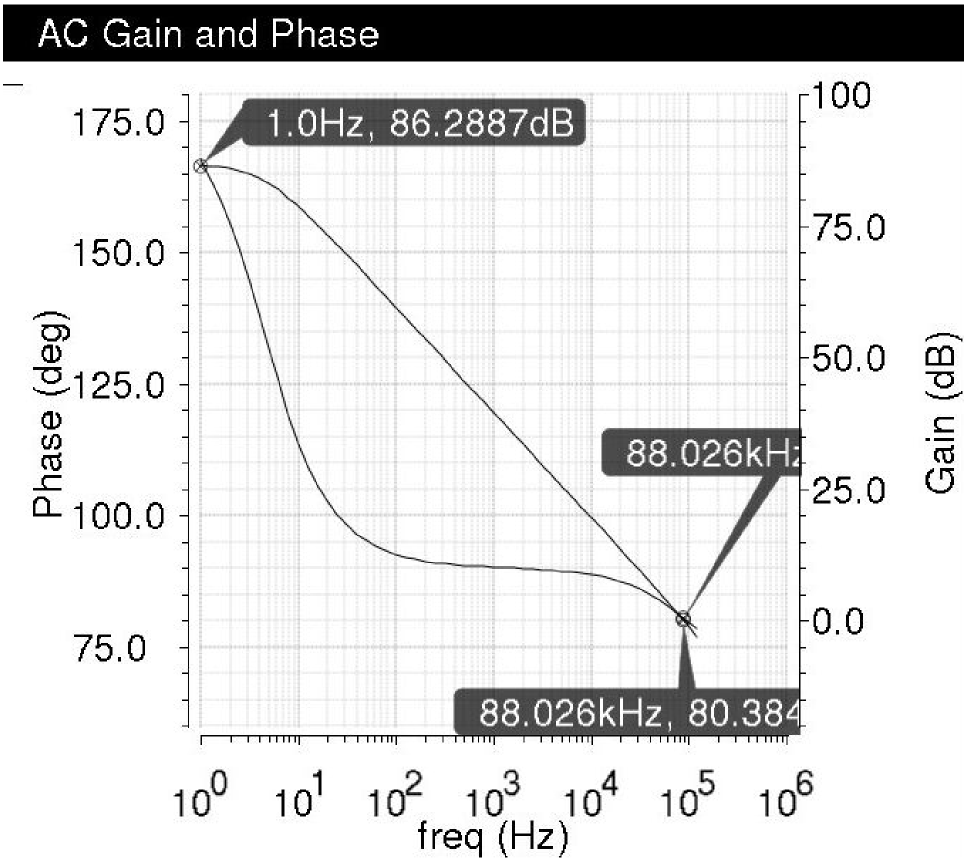


Fig. 3.22: AC gain and phase.

negligible. Thus, the settling time is almost the same as in pre-layout simulation.

In contrast, with the settling time, the maximum *INL* and *DNL* have increased visibly. The parasitic resistance of wiring metals has dramatic influence on the linearity of the low voltage DAC. Besides, the mismatch of the input pair in the amplifier caused by the parasitics results in offset error as well. *INL* and *DNL* based on the post-layout simulation result are shown in Fig. 3.25 and Fig. 3.26. The maximum *INL* and maximum *DNL* are $0.42\ LSB$ and $0.35\ LSB$ respectively. The offset error is $182\ mV$, and the gain error is $0.42\ LSB$.

3.3.4 Corner Analysis and Monte Carlo Simulation

Due to process inaccuracies, temperature and parameter variations, the circuit's performance could have deviations while being measured. To guarantee the yield of the *ASIC*, corner analysis and Monte Carlo Simulation are used to estimate the impact of the extreme manufacturing variations on the circuit's performance.

Corners that describe the variations during the fabrication process are supplied with the design kit by IC foundries. In *AMS* design kit, the worst slow (*WS*), the worst power (*WP*), the worst one (*WO*), the worst zero (*WZ*) and typical section are available in mod-

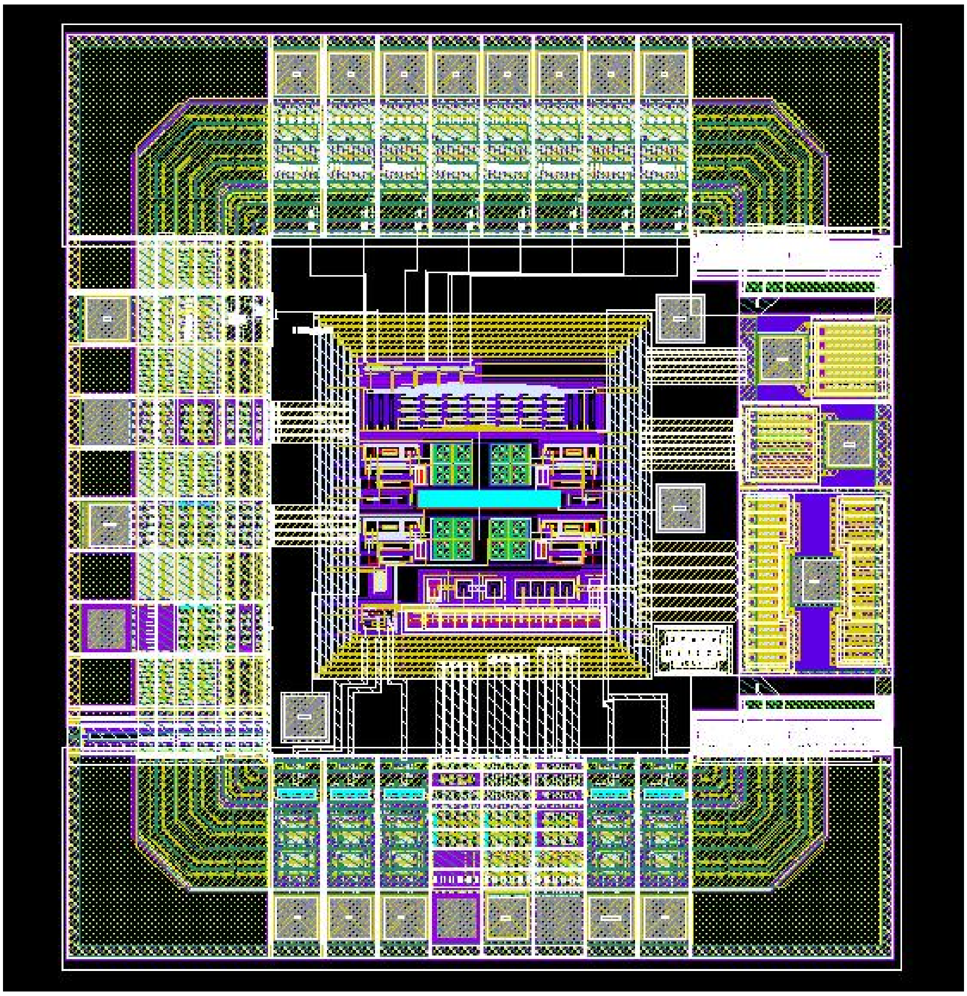


Fig. 3.23: Layout of the high voltage digital to analog converter for reconfigurable antenna array.

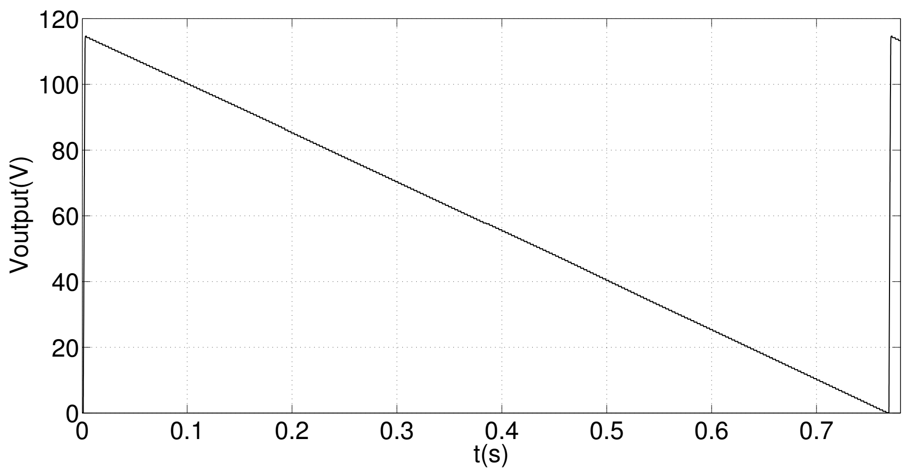


Fig. 3.24: Post-layout simulation result of the output voltage.

els library. Besides these process variation, the corners are also possible to describe the circuit's performance in different temperatures and other parameter variations. For ex-

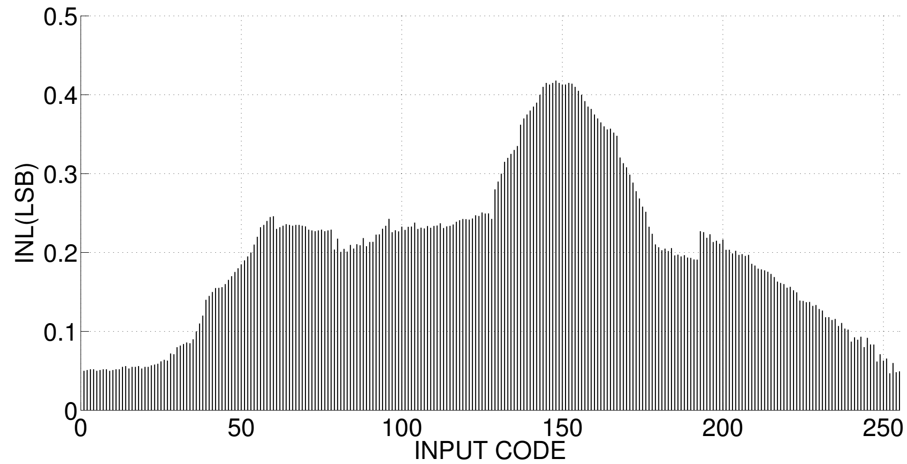


Fig. 3.25: INL of the high voltage DAC in post-layout simulation.

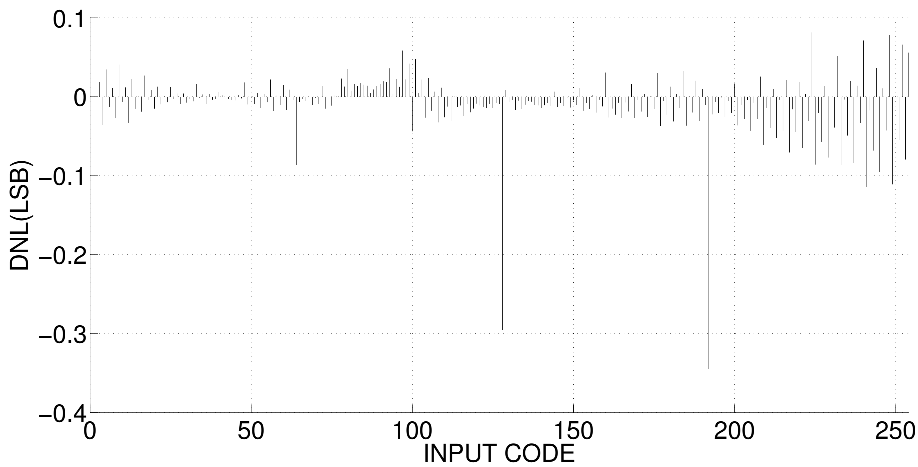


Fig. 3.26: DNL of the high voltage DAC in post-layout simulation.

ample, when power supply (Vdd) is a variable in schematic, it can be simulated as a parameter variation in corner analysis. In *ADE XL*, each corner can be simulated with device corner models, temperature or other various parameters. The possibility that all requirements will be met during chip measurement increases while a design meets all specifications in corner simulation.

In this design, circuit devices have four corner sections(*WS*, *WP*, *WO* and *WZ*). Low voltage power supplies will be given by DC voltage generator or batteries. High voltage power supply is provided by a charge pump which can generate $115\ V$ from a battery. Since the output voltage of the charge pump is affected by process variations, load resistance and environmental conditions such as temperature, it has to be taken into account in corner analysis. The duty circle of the 4-phase clock in the charge pump can be adjusted by a feedback loop controlled by a micro controller. With this calibration circuit, the output voltage range of the charge pump is stabilized between $114\ V$ and $115\ V$. According to our application, $-20\,°C$ to $100\,°C$ is selected as the temperature range.

To ensure the circuit performance, it should be simulated with different combinations of variable parameters. Simulating all combinations will consume much time and increase the design period, especially for complicated circuits with many variable parameters. In order to shorten the simulation time, a better solution is to choose reasonable worst corners instead of simulating all possible corner combinations.

In our specific application, required biasing voltage of the functional material is only $90\,V$. Therefore, the deviation of maximum output voltage is not the most important specification. Because of the limited load current provided by charge pump and the relatively high value of the input capacitance, the slow rate variation has a primary influence on the system performance. To test the influence of variable parameters on the slow rate, the simulation is performed by sweeping only one parameter.

Fig. 3.27 and Fig. 3.28 shows the simulation result in variable temperatures. In this simulation, the power supply is set to $115\,V$, *WP* and *WZ* are selected as the device model section, respectively. Based on the simulation result, it is proven that the slow rate decreases by increasing temperature. The maximum output voltage and the voltage step also decrease because of the lower value of on chip resistance.

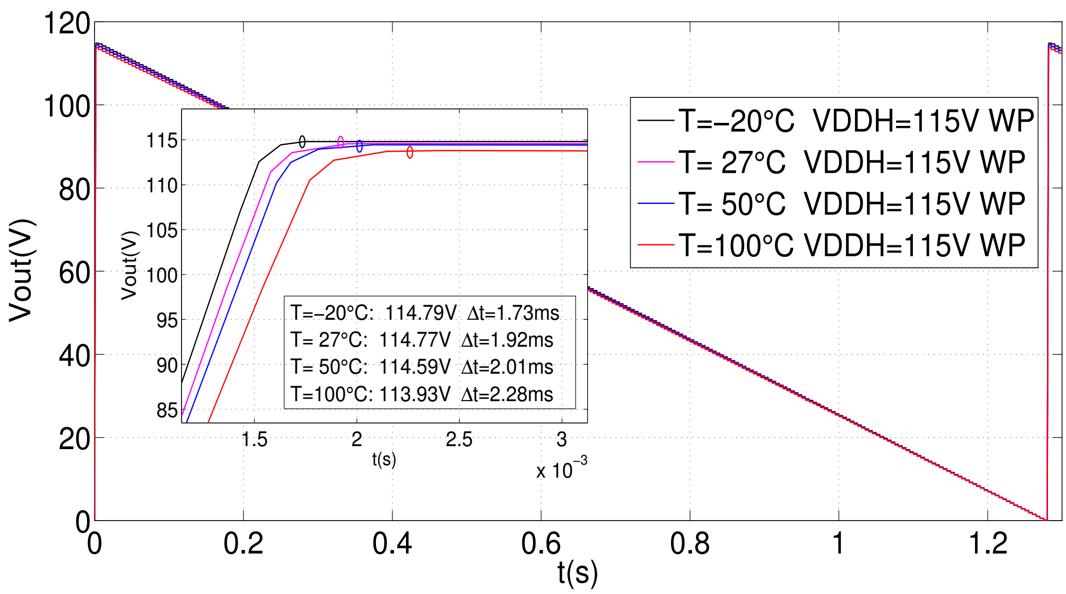


Fig. 3.27: Simulation result of corner analysis with variable temperatures (power supply: 115 V, device model section: WP)

Fig. 3.29 and Fig. 3.30 shows the simulation result of corner analysis with different device models. In this simulation, the power supply is set to $115\,V$, the temperature is set to $27\,°C$ to $100°C$ respectively. According to the simulation result, the maximum slow rate is achieved with *WP* device model section, and the minimum slow rate occurs with *WS* device model section. The order of the output voltage from high to low is *WO*, *WP*, *WS* and *WZ*.

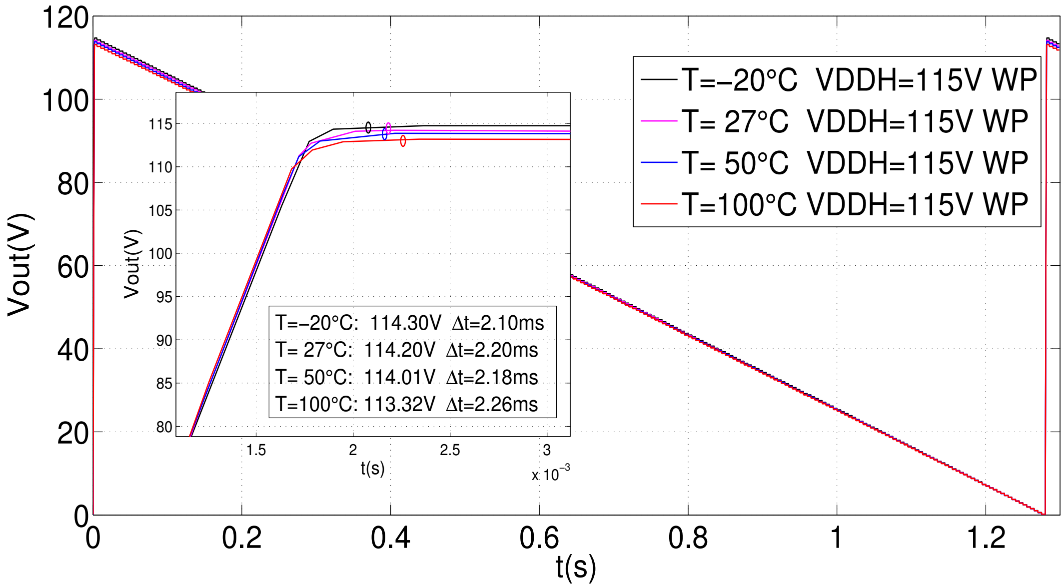


Fig. 3.28: Simulation result of corner analysis with variable temperatures (power supply: 115 V, device model section: WZ)

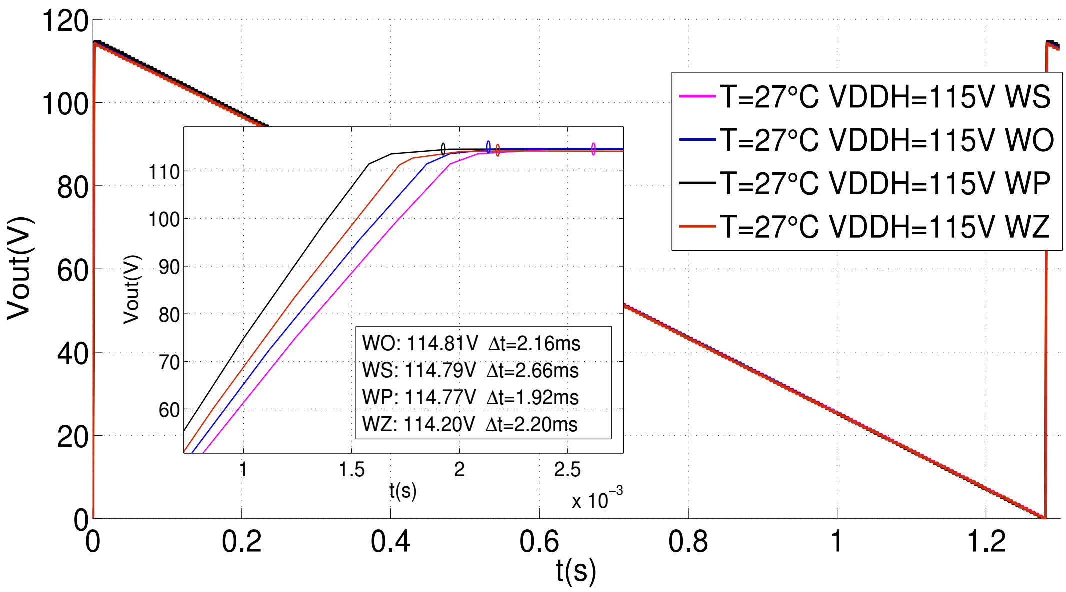


Fig. 3.29: Simulation result of corner analysis with different device model sections (power supply: $115\ V$, temperature: $27\ °C$)

Based on the simulation results above, it has been proven that the minimum slow rate could be achieved with the lowest temperature and *WS* device model section. Therefore, eight parameter combinations in Tab. 3.1 are selected to perform the corner analysis. Fig. 3.31 shows the simulation result of corner analysis. According to it, the lowest and the highest slow rate are $38.22\ V/ms$ and $70.68\ V/ms$, respectively.

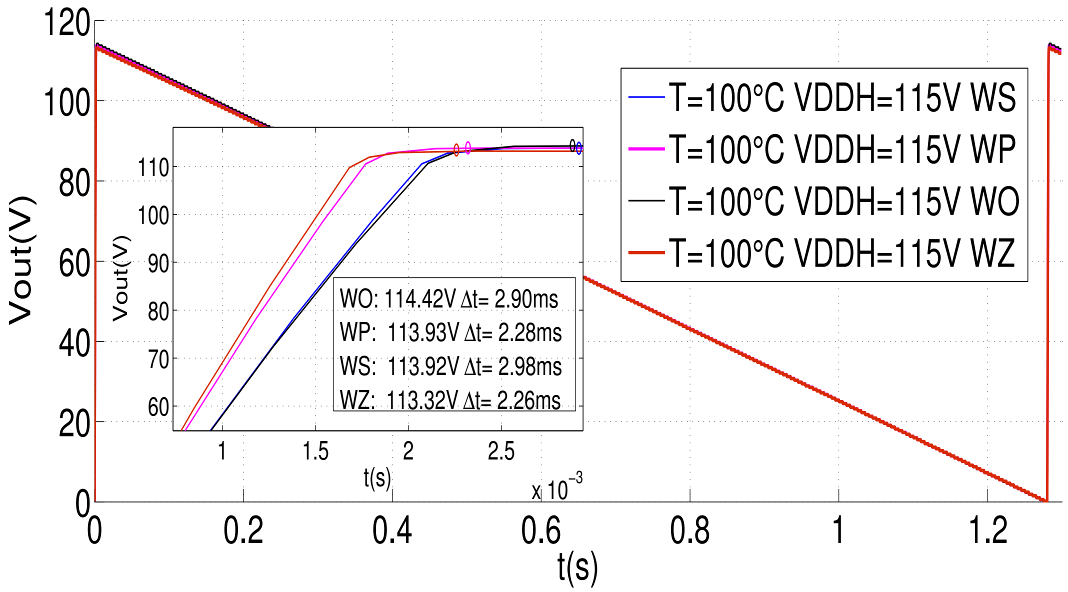


Fig. 3.30: Simulation result of corner analysis with different device model sections (power supply: $115\,V$, temperature: $100\,°C$)

Tab. 3.1: Parameter combinations in the corner analysis

Power Supply(V)	Temperature($°C$)	Device Model Section
114	-20	WP
114	-20	WS
114	100	WP
114	100	WS
115	-20	WP
115	-20	WS
115	100	WP
115	100	WS

The tunable *RF* devices applied by functional material such as liquid crystal doesn't have a high switching speed. Therefore, even in the worse corner, the speed can fulfill the requirement in this application. This simulation is carried out with a load capacitance of $800\,pF$ including the input impedance and off-capacitance of high voltage switch array. If the high voltage switch is eliminated or implemented on chip, the speed of the *HV DAC* will be greatly improved.

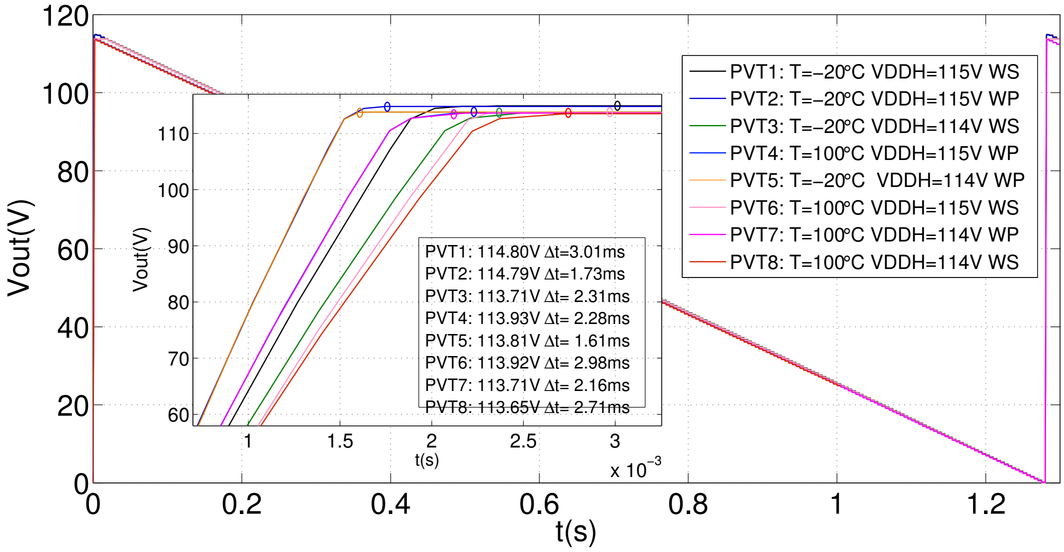


Fig. 3.31: Simulation result of corner analysis

3.4 Experimental Results for "Aries"

The circuit design was fabricated by *AMS* foundry in November 2012. The unpackaged *ASIC* was amounted on an empty chip socket. The chip photos are shown in Fig. 3.32.

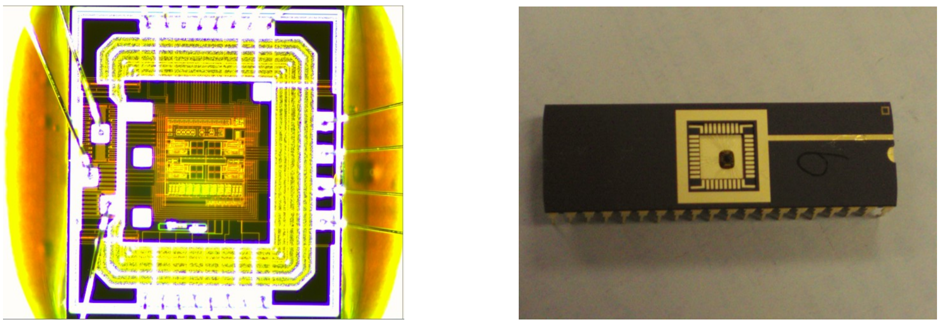


Fig. 3.32: The chip photo under microscope and packaged ASIC

Experimental *INL* and *DNL* are determined based on the measured output voltage. Because of process and mismatch variations during fabrication, *INL* and *DNL* in experimental test are larger than the post simulation result. The maximum *INL* is $0.48\ LSB$ and the maximum *DNL* is $0.38\ LSB$ as shown in Fig. 3.33 and Fig. 3.34. Besides the high voltage amplifier and the low voltage *DAC*, other circuit blocks are also integrated in this chip to provide bias voltages and protect low voltage devices. The total power consumption of the chip is less than $18\ mW$.

The speed of this *DAC* depends on the input capacitors of the tunable device. Since this chip is powered with a high voltage power supply generated by a charge pump, the load current is quite limited. Therefore, the speed of this *DAC* is dominated by the

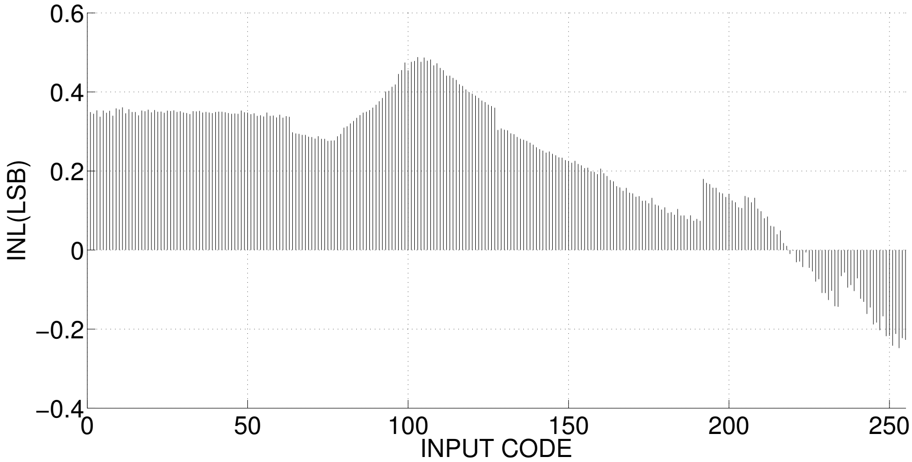


Fig. 3.33: INL of the high voltage DAC in experimental measurement.

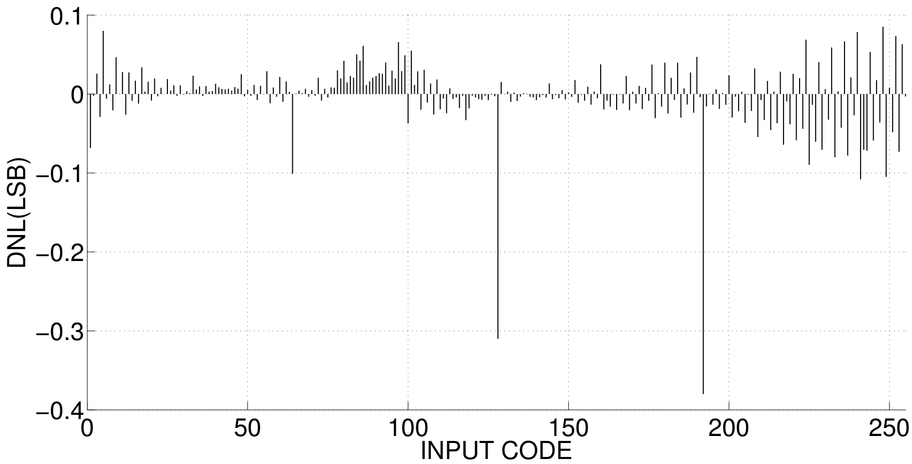


Fig. 3.34: DNL of the high voltage DAC in experimental measurement.

required charging time for the load capacitor (input impedance of antenna). The maximum input capacitance of the antenna is $20\,pF$. To test the speed in this worst case, the charging time is measured with a $800\,pF$ load capacitor(the sum of input capacitance and off-capacitance of high voltage switch array). Due to process and mismatch variations, the measured charging time of one channel from 0 to $115\ V$ varies between $1.9\ ms$ and $2.5\ ms$ within the result of the corner simulations. Since the switching speed of tunable devices in our application is not high, the speed of this *DAC* can fulfill the requirement of the application.

To compare with previous publications [HC12] [SMP05], the measurement result in this work and the specifications of other published designs are summarized in Tab. 3.2. High voltage *DAC* is a relatively new field in *ASIC* design, the previous works hence are quite limited. Most designs are in very old technologies and provide different output voltage ranges from our design. These two selected *ASICs* are designed for other applications, but have the most similar specification to our design. Unfortunately, the experimental result and some important performance are not mentioned in these publications as shown in this table.

Tab. 3.2: Comparison with previous designs

	[HC12]	[SMP05]	Aries
Technology	0.25 μm	0.8 μm	0.35 μm
Output Voltage Range(V)	0-60	0-300	0-115
Resolution	10-bits	6-bits	8-bits
DNL(LSB)	0.003 (simulation result)	0.16 (simulation results)	0.38 (measurement result)
INL(LSB)	0.28 (simulation result)	0.18 (simulation result)	0.48 (measurement result)
Chip Area(mm^2)	2.9279	not available	3.5
Power(mW)	not available	not available	18

To prove the concept of the whole system, a demonstrator is built to test the system performance. This demonstrator consists of a dual-band antenna, a charge pump and two digital to analog converters proposed in this chapter. The description of the demonstrator and the experimental test result will be introduced in chapter 5.

Chapter 4

Second ASIC: An Integrated High Voltage Controller with a DAC Array

Contents

4.1 System Overview

The high voltage *DAC* with single output proposed in chapter 3 has proven the feasibility to use *HV ASIC* in communication systems. But external switches are required as using this *ASIC* to apply individual voltages for multi-channel in antenna arrays. If multi-output functionality can be implemented on chip, it will greatly reduce the size and the complexity of the high voltage controller, and significantly increase the hardware integration density of portable devices. The proposed high voltage controller design (”Taurus”) in this chapter is mainly based on my own publication [NH14].

4.1.1 Requirement Analysis

Two common solutions are available to fulfill the multi-output requirement of the application. We can implement either high voltage switches or multi-DACs on chip to provide different voltages for individual channels in antenna arrays. Chip size, cost and performance have to be analyzed to choose a better solution.

4.1.1.1 High Voltage Switch Design

Fig. 4.1 shows the basic structure of conventional transmission gate. A and $\bar{A}$ are control signals to switch on/off the transmission gate. The transmission gate is open and closed, respectively, as the transistors working in cut off region and saturation region.

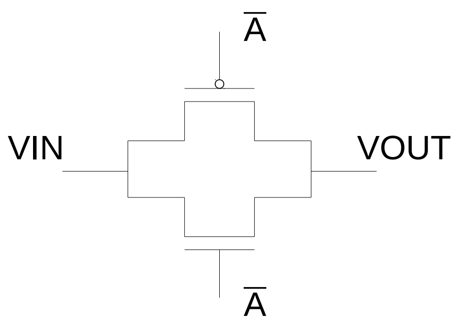


Fig. 4.1: Transmission gate

For this application, the voltage difference between source and control signal could reach $120\,V$. High voltage transistors with the thickest oxidation layer could be damaged as V_{GS} exceeding the safe operation area. Thus, conventional transmission gate are not suitable for this application, and extra circuits are required to protect the devices in the high voltage switch.

4.1.1.2 Over Voltage Protection Circuit

To avoid exceeding the safe operation voltage area, over voltage protection circuits are required to limit gate to source voltage of the transistors in the high voltage switches. Fig. 4.2 shows the principle of the protection circuit.

Due to the voltage requirement of the application, VIN and $VOUT$ should be in the range of $0\ V$ to $120\ V$ and could lead to violation of *SOAC* for V_{GS} of the *PMOS* switch

($P1$). To avoid the violation, a series of diode connected $PMOS$ transistors($P1$ to PN) are used to limit the gate to source voltage.

The $NMOS$ transistor $M1$ is turned off while $VCTRL$ is low. In this case, there is no current flowing through the diode connected transistors, and the resistor $R2$ pulls the gate voltage of $P0$ to VIN. When the control voltage $VCTRL$ is set to high, the PMOS switch will be turned on. The gate voltage V_{G0} will be pulled towards VSS when I_{REF} is zero. When I_{REF} increases, V_{G0} will be blocked as $VIN - nV_{TH}$. Therefore, the $PMOS$ switch $P0$ is protected by fixing the gate to source voltage less than nV_{TH}.

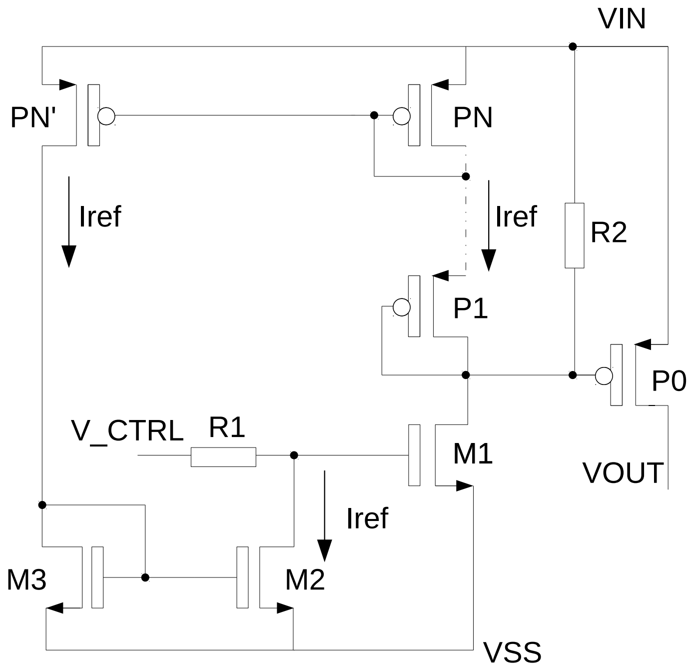


Fig. 4.2: Over voltage protection circuit

In our application, the input voltage range of the high voltage switch is from $0\ V$ to $120\,V$. Thus, VSS must be lower than $0\,V$ to turn on the switch and transfer input voltage close to $0\ V$, which requires generating a negative voltage on chip and will definitely increase the complexity and the area of the high voltage switch. Each high voltage switch occupies more than $1\ mm^2$ on chip. Moreover, this over voltage protection circuit will consume some current from high voltage power supply which is not acceptable due to the current limitation of the charge pump in the system. Hence high voltage switches are not suitable for this application, and we need to find another solution to provide multiple outputs.

4.1.1.3 Analysis of Multi-DAC Design

A high voltage *DAC* array is another option to provide multiple individual outputs with different voltages. The same as the first chip design, the most important specifications are cost, chip size and power consumption. According to the proved design in chapter 3, the topology with a low voltage *DAC* and a high voltage amplifier is reused in the new design proposed in this chapter. High voltage transistors are only used in the high voltage amplifier which consumes most area of the chip. The size of the designed high voltage amplifier is $0.25\ mm^2$, and the current consumption from high voltage power supply is $80\ \mu A$. Compared to the high voltage switch, this solution doesn't require any negative voltage on chip, and it consumes less area and power consumption from the high voltage power supply.

4.1.2 Structure of the high voltage DAC array

Based on the requirement analysis, high voltage *DAC* array is selected to be implemented to provide high voltages for different channels in antenna arrays. To control the *DAC* array with multiple outputs, a simple digital controller is required to store and transfer the digital inputs and synchronize the outputs. Thus, the high voltage *DAC* array should be composed of a low voltage digital controller and 16 high voltage digital to analog converters as shown in Fig. 4.3.

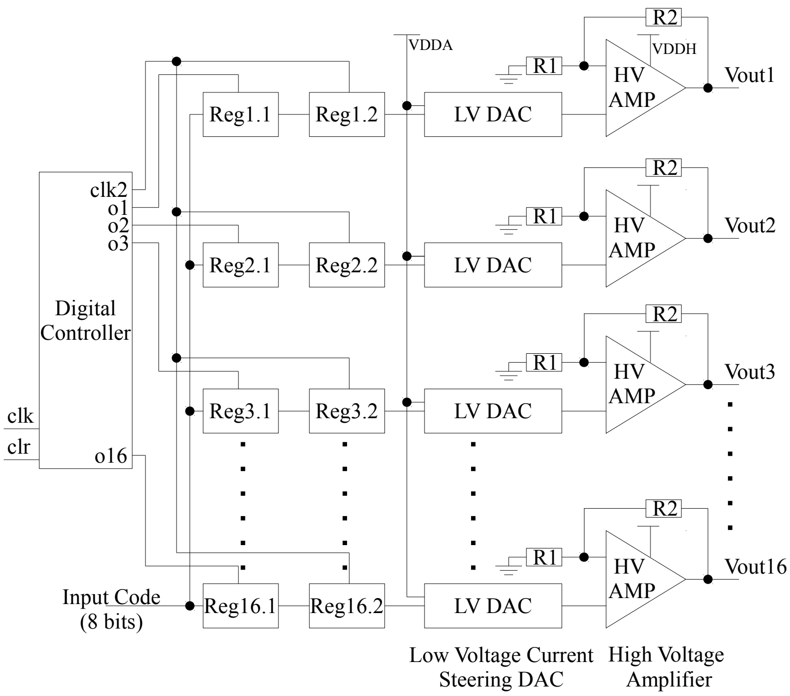


Fig. 4.3: Structure of the high voltage DAC array

To achieve the required high voltage and reduce the chip area, each *HV DAC* mainly consists of a low voltage *Current Steering DAC* to provide 256 voltage steps and a high voltage amplifier to boost the voltage up to $120\ V$. As introduced in Chapter 3, even in the high voltage amplifier, only a few high voltage transistors are used to stand with the high voltage and protect the other transistors from breaking down. By using this topology, both chip size and power consumption can be significantly reduced. Furthermore, comparing with a single high voltage *DAC*, this topology consumes smaller current from the high voltage power supply and has more accurate outputs.

4.2 Design Implementation

In this section, the concept and schematic of the low voltage *DAC*, the high voltage amplifier and the small digital controller will be described in details, and the pre-layout simulation results will also be presented.

4.2.1 Low Voltage DAC

As discussed in Chapter 3, *DACs* are the interface between analog and digital circuits. Many topologies (e.g. *Binary-weighted DAC*, *Delta-sigma DAC*, *R2R DAC* etc.) are used for different applications. To achieve high voltage above $100\ V$, the *ASIC* has to be implemented in high voltage technology. Thus, the low voltage *DAC* is built by using transistors with isolation layers as well. Comparing to low voltage technologies, devices of the selected technology (*AMS H35*) shows worse characteristics than those in low voltage technologies. Due to their complicated structures, they have larger leakage current, more parasitics and larger size, which have non negligible impact on performances of the proposed *DAC*. Since the requirement of frequency for antenna arrays, which are fabricated by using liquid crystal, is relatively low(only few kilo Hertz), the relatively low switching speed of devices in this technology is acceptable. This circuit is designed for portable devices and mobile applications, hence it needs to be powered by a battery, and low power consumption becomes an important requirement to be fulfilled. Considering accuracy, power consumption and chip size, the current steering topology is chosen to design the low voltage *DAC*. Be different from *Transistor Only R2R DAC* implemented in the first chip, it eliminates the negative power supply and is able to operate in the maximum voltage range($0\ V$ to $120\ V$) provided by *AMS H35*.

4.2.1.1 Current-Steering DAC Design

The current steering *DAC* it the most frequently used topology in communication applications, because it is suitable for high speed applications and possible to be calibrated to achieve relatively high resolution [AAVW04, AV04, SAV04]. This architecture is based on the switched-current technique [SVA04] as shown in Fig. 4.4.

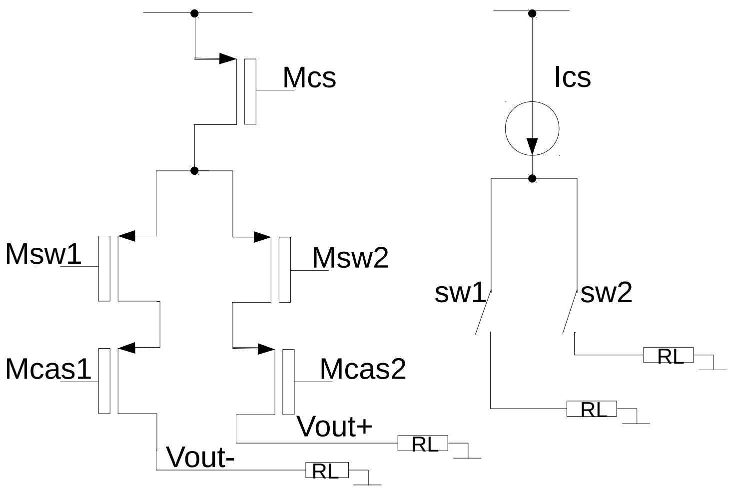


Fig. 4.4: Basic PMOS current steering unit cell

The current is delivered by an ideal current source which is independent of the voltage drop. In this figure, a current source is implemented with a $PMOS$ transistor (Mcs) which is biased in saturation region. The output resistance of the current source is:

$$R_{out} = \frac{1}{g_{ds}} \tag{4.1}$$

A differential current switch is implemented with two *PMOS* transistors ($Msw1$ and $Msw2$). If both switch transistors are simultaneously switch off, charge will be accumulated at the output node and lead to high energy glitches in the transient response as one transistor starting to switch on. Therefore, when the differential switch changes its state, it is important to prevent two transistors being cut off at the same moment. When calculating the output resistance of the unit current cell, the output resistance of the switch should also be taken into account. To increase R_{out}, additional cascade transistors ($Mcas1$ and $Mcas2$) are connected with the switch in parallel. For high frequency application, the output impedance is normally limited by capacitive parasitics which is not considered in our design.

Binary weighted current steering *DAC* requires N current source unit for N-bits *DAC* to generate $2N - 1$ current or voltage steps at the output as shown in Fig. 4.5. This architecture can be implemented with binary weighted current mirror. The huge size ratio of the transistors in the current mirror could result in mismatch problem and reduce the output accuracy. To solve this problem, $W2W$ topology as shown in *LSB* part in Fig.4.6 is selected to replace the binary weighted structure. The high leakage and big mismatch and process variation could cause the worse performance than *DACs* designed in low voltage technology. Thus, the proposed *DAC* in this design is implemented in segmented structure to ensure the resolution requirement of the application.

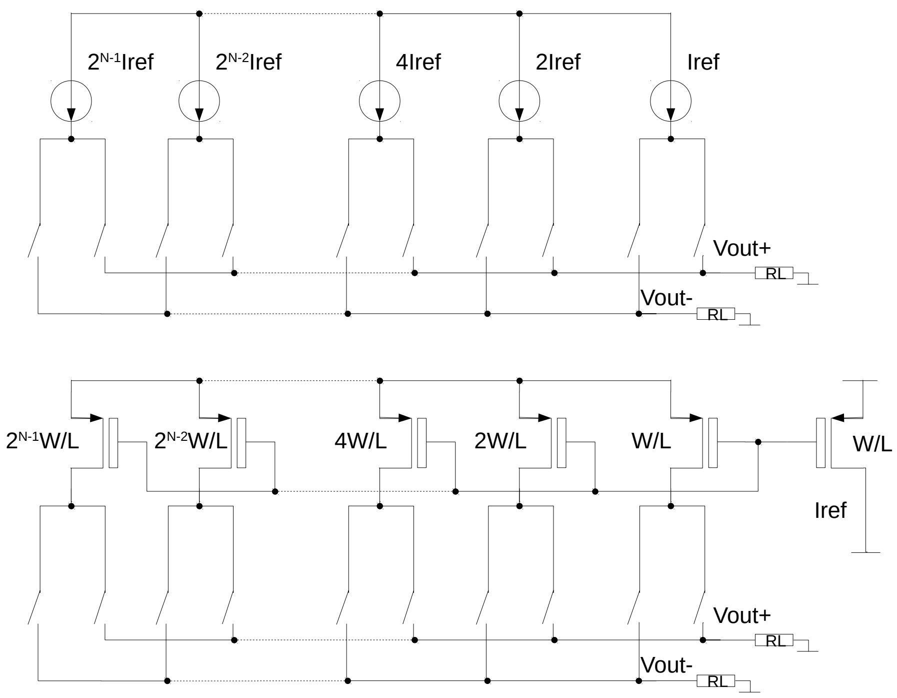


Fig. 4.5: Binary weighted current-steering DAC and binary weighted current-mirror

This segmented current-steering *DAC* consists of two sub-DACs to reduce the performance lose caused by high glitch energy and mismatch variations during fabrication. Thus, this segmented topology could lead to better linearity and accuracy of the data conversion. The six least significant bits and two most significant bits steer a unary and a binary current array, respectively. In this *DAC*, all resistances of R2R topology are replaced by transistors with the same aspect ratio (W/L) to improve integration density of the chip. An unit current cell of the binary array is shown in the dashed rectangle in Fig. 4.6. Transistors in series ($M1$ and $M2$, $M5$ and $M6$) can be viewed as two equivalent transistors with an aspect ratio equals to $W/(2L)$. The unit cell composed of these two equivalent transistors in parallel can be viewed as a transistor with an aspect ratio equals to W/L. This W2W structure exits in each current cell of the unary weighted current array. Thus, all current of other unit cells is a factor of 2^n greater than the *LSB* current cell, where n is the bit number. The differential switches (e.g. $M7$ and $M9$) are used to keep the same voltage drop across the switches when they are on or off. As shown in Fig. 4.6, two cascade transistors(e.g. $M7$ and $M8$) are used for each differential switch to increase the output resistance of the current source. All transistors in this *DAC* are biased in deep saturation region. To reduce the influence caused by process variation, a bandgap reference is designed to provide a reference current for the current mirror.

The size of the transistors depends on the specification of the *DAC* and the mismatch properties of the devices in this technology. The minimum size (WL) of transistors are

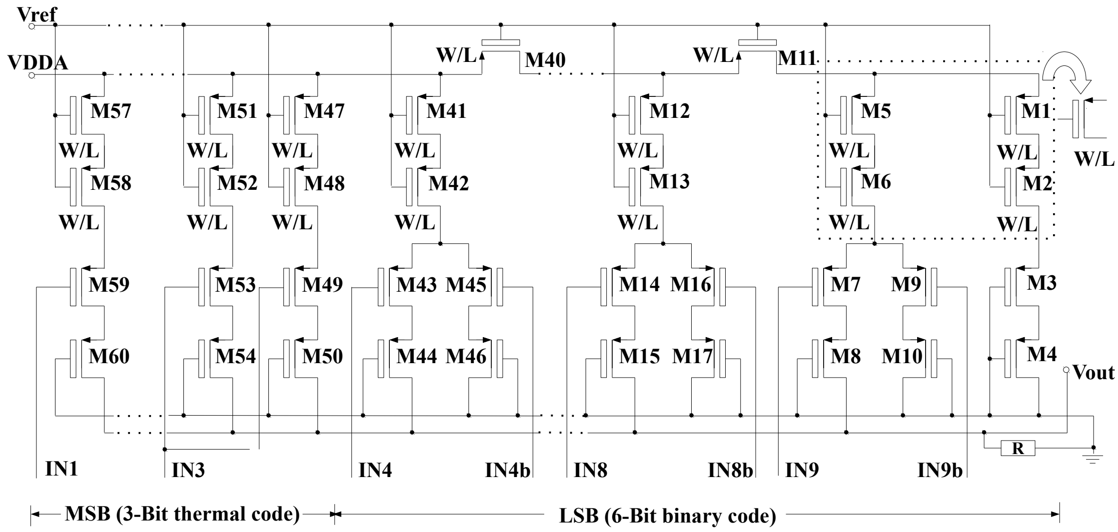


Fig. 4.6: 8-bits segmented low voltage current-steering DAC

calculated by using following equations [PDW+89, VdBSS01].

$$INL = \sqrt{2^{(N-2)}}\frac{\sigma I}{I}(LSB) \tag{4.2}$$

$$DNL = \sqrt{2^{(N'+1)} - 1}\frac{\sigma I}{I}(LSB) \tag{4.3}$$

$$(WL)_{min} = \frac{[A_\beta^2 + \frac{4A_{vto}^2}{(Vgs-Vth)^2}]}{2(\frac{\sigma I}{I})^2} \tag{4.4}$$

N is the number of bits. N' is the number of unary unit cells. To fulfill the requirement of the application, both *INL* and *DNL* must be less than one *LSB*. A_β^2 and A_{vto}^2 are matching parameters of the transistors. By using *INL* yield equals to 99.7%, the minimum gate area (WL) is $16\ mm^2$. Considering the minimum size and W/L ratio, $9\ \mu m/3\ \mu m$ is selected as the aspect ratio to build the *DAC*.

This *ASIC* is designed for mobile applications and has to be powered by a battery. The power consumption hence becomes the biggest challenge. The maximum current of the *DAC* is $250\ \mu A$ and the power consumption of the *DAC* is less than $1.25\ mW$.

4.2.2 High Voltage Amplifier

Besides the low voltage part, a high voltage amplifier is also required for each channel to boost the voltage up to $120\ V$. In our previous work [NH13], a two stage *HV* amplifier, which can provide high voltage output up to $115\,V$, has been implemented. The structure given in Fig. 4.7 has already been proved by experimental test in chapter 3.

4.2.2.1 High Voltage Amplifier Architecture

As introduced in chapter 3, the *HV* amplifier is designed using a two stage miller-compensated operational amplifier. The structure is reused in the second chip.

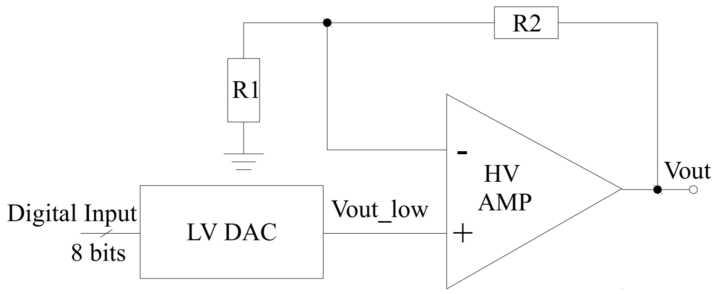


Fig. 4.7: The structure of each channel in the high voltage DAC array

To reduce the chip area, the first stage is designed by using LV transistors and HV transistors are only used to build the second stage to block high voltages. The chip area and power consumption are greatly reduced by using this topology. As shown in Fig. 4.8, only six *HV* transistors are used in the amplifier.

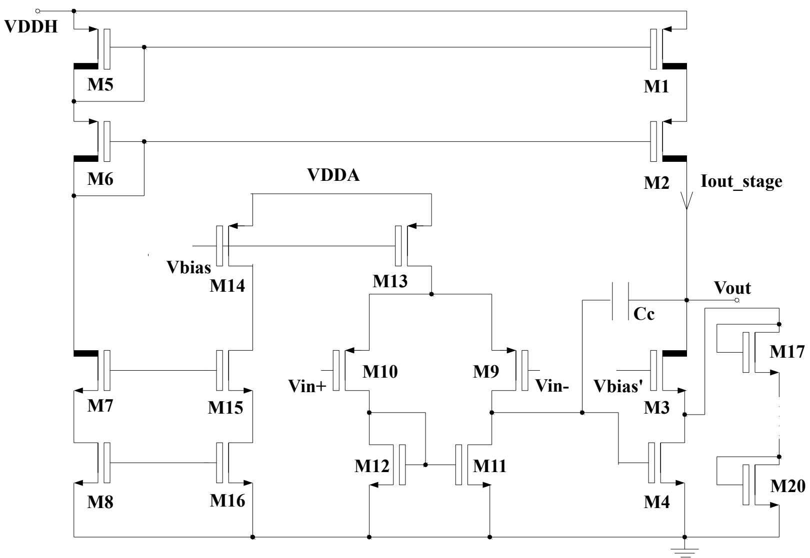


Fig. 4.8: The structure of the high voltage amplifier

Since the output voltage range is from $0\ V$ to $120\ V$, at least four *HV* transistors ($M2$, $M3$, $M6$ and $M7$) are required to block high voltages. The statistic current of the high voltage stage is provided by two current mirrors ($M1$ and $M5$, $M8$ and $M16$). The maximum V_{GS} and V_{DS} of the four transistors in the second stage ($M1$, $M2$, $M5$ and $M6$) will not exceed $5\ V$, when the bias current is sufficiently low. To generate more accurate current and to save area, these current sources should be built by *LV* transistors. However they can not be replaced by *LV* because of the voltage limitation between drain and p-substrate ($50\ V$). Furthermore, four *LV* transistors in series are used to protect the drain source voltage of $M14$ exceeding the safe operation area ($5\ V$).

The second stage is powered by $120\ V$ power supply, the statistic power consumption of this amplifier hence depends mainly on the bias current of this stage. To fulfill the power consumption requirement of mobile devices, the current has to be sufficiently low. Because this amplifier provide a driving voltage (from $0\ V$ to $120\ V$) for a channel in antenna arrays, the driving ability has to be considered. The input impedance of the antenna array is purely capacitive, and the maximum capacitance is around $20\ pF$. Furthermore, the materials used to implement tunable antennas like liquid crystal do not require high switching speed. Thus, a relatively low current in the output stage is possible to fulfill the requirement of the driving ability. To increase the slew rate of the circuit, W/L ratios of $M1$ and $M5$ should be adjusted to achieve higher current in the output stage. In this amplifier, the bias current of the output stage is 70μA, and the total current consumption from VDDH is only 80μA. The power consumption of the amplifier is $9.7\ mW$. As the voltage controller with 16 channels consuming only $1.28\,mA$ from VDDH, it is possible to be powered by a high voltage power supply generated by a charge pump.

Due to low statistic current of the output stage, the driving ability of the amplifier is week. As shown in Fig. 4.7, the feed-back loop($R1$ and $R2$) used to boost the output voltage consumes current from the output stage as well. It has important impact on slew rate of the output stage. Thus, the feed-back resistors must be sufficiently large to reduce the required current. The full-scale output can be calculated by the following equation:

$$V_{out} = \frac{(R1 + R2)}{R1} V_{out\_low} \tag{4.5}$$

In this circuit, the output voltage coming from the *LV DAC* is in the range of $0\ V$ to $2\ V$. $R1$ equals to $0.1\ M\Omega$, $R2$ equals to $5.9\ M\Omega$, and the maximum output voltage of the amplifier is $120\ V$. With the full-scale voltage, the maximum current consumption of the feed-back loop is $20\ \mu A$. In the worst case, with the maximum input capacitance ($20\,pF$) of each channel in the antenna array, it takes $0.1\ ms$ to reach $120\ V$ from $0\ V$.

4.2.2.2 Pre-layout Simulation of High Voltage DAC

Be different from the first chip, this chip can provide 16 individual output without external switches. Thus, the simulation should be carried out with input impedance of each channel in antenna arrays. In our application, the input impedance of the antenna is from $10\ pF$ to $20\ pF$. The raising time of the output voltage is dramatically reduced with the load capacitance of $20\,pF$.

Though we have 16 *HV DACs* on chip, the output difference and gain error could not be observed in pre-layout simulation result because the parasitics are not taken into account during simulation. It will be discussed based on the post-layout simulation in section 4.3. In pre-layout simulation, the 16 channels have the same performance (e.g *INL*, *DNL* and offset error) as shown in Fig. 4.9 and Fig. 4.10.

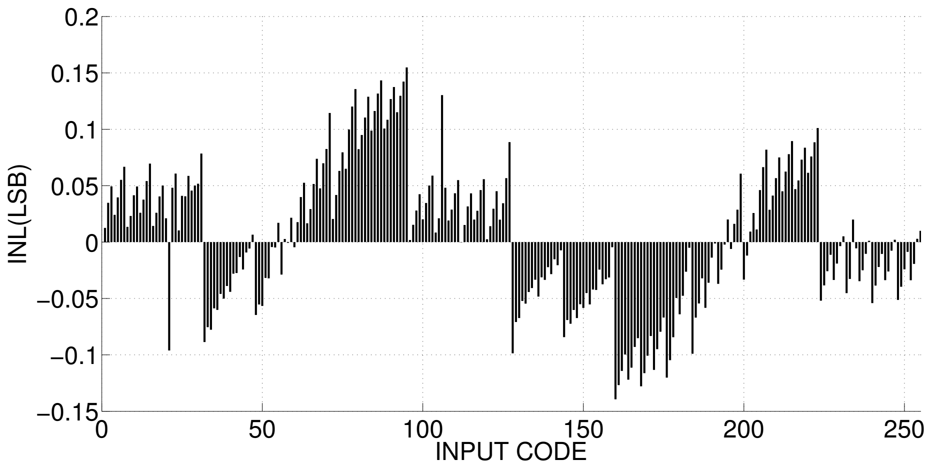


Fig. 4.9: INL of the high voltage DAC in pre-layout simulation.

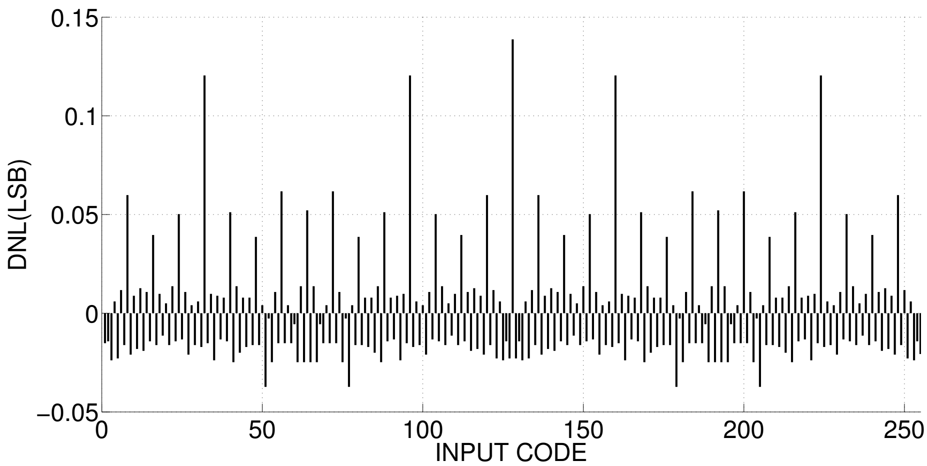


Fig. 4.10: DNL of the high voltage DAC in pre-layout simulation.

4.2.3 Digital Controller

The digital part on chip is used to control data transfer, to divide input clock frequency and to synchronize multi-outputs. As shown in Fig. 4.3, the registers in the first column controlled by a digital encoder are used to store the input data and the registers in the second column are controlled by the output (CLK2) of a 4-bits counter in the digital controller to store the coming input signals as shown in Fig. 4.11. After 16 clock periods, all input patterns will be stored in these registers. As the rising edge of CLK2 coming, these registers will be synchronously refreshed. Then the output voltages of the 16 channels will be synchronously changed.

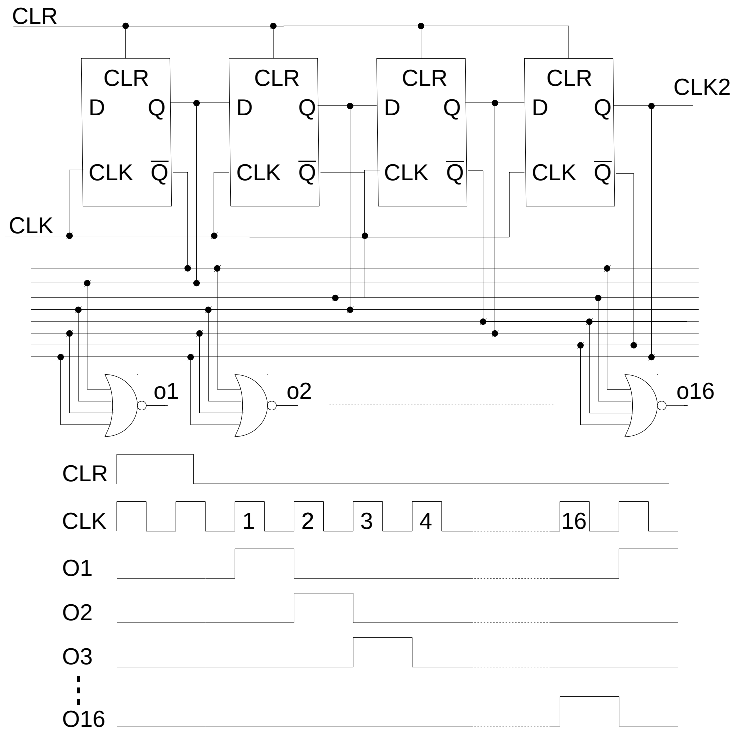


Fig. 4.11: The on-chip digital part for controlling the 16 outputs.

4.3 Chip Fabrication: "Taurus"

As discussed in Chapter 3, compared to designs in low voltage technology, the performance of high voltage technology designs will be much worse because of the sophisticated physical, parasitics and high leakage current. Since there are 16 channels in this design and the feedback resistors are also implemented on chip, layout quality will have significant impact on the performance.

4.3.1 Layout of the Low Voltage DAC

Compared to transistors used as differential cascade switches, current steering transistors with the same aspect ratio of W/L have more impact on the accuracy of the low voltage *DAC*. Thus, these transistors are divided into small devices and connected as shown in Fig.4.12 to reduce the mismatch caused by different boundary condition, parasitics and process variations to achieve a better accuracy. Moreover, the *LSB* unit are put in the middle of the layout, and the rest unit cells are placed from the middle to the margins in order.

To prove the functionality and the performance of this circuit block, post-layout simulation is carried out with extracted file.

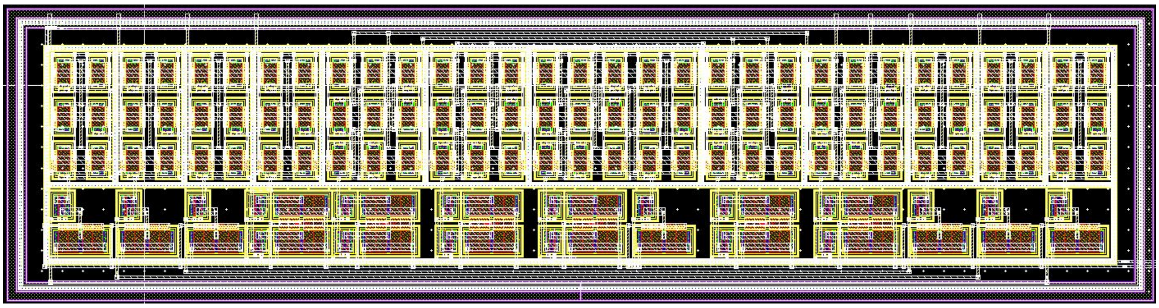


Fig. 4.12: Layout of low voltage current steering DAC

4.3.2 Layout of the High Voltage Amplifier

Instead of the $115\ V$ high voltage amplifier, a *HV* amplifier which can boost the input voltage up to $120\,V$ is designed in "Taurus". Besides, in this design, the feedback resistors and compensation capacitor are also implemented on chip. Since the *HV DAC* will be duplicated to implement the *DAC* array, the area of *HV DAC* unit must be evaluated. The size of *HV DAC* layout unit including *LV DAC*, *HV* amplifier and registers is $0.25\,mm^2$ as shown in Fig. 4.13.

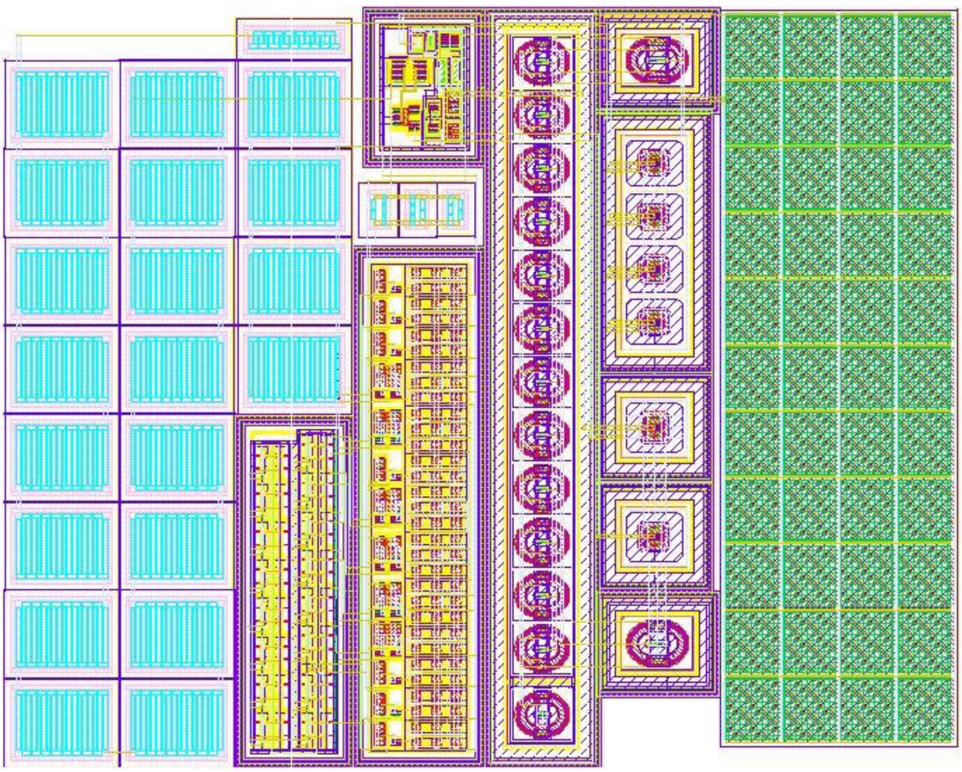


Fig. 4.13: Layout of high voltage DAC unit

4.3.3 Post-layout Simulation Result of "Taurus"

Due to the complex physical structure of *HV* devices, layout of high voltage *SOCs* is more sophisticated than low voltage technologies. High voltage devices are much larger than low voltage devices because of their isolation layers, extra drift region and thick oxidation layer. Furthermore, to reduce leakage current and latch-up, guard ring has to be added to surround each high voltage transistor. In addition to large devices, metal layers, spacing between different layers and other devices in *HV* technology are larger than those in *LV* technology as well. The size of high voltage chip is hence usually relatively larger than low voltage ones.

The layout of the proposed high voltage *DAC* array is shown in Fig.4.14. High voltage pads including large *ESD* protection devices take most area of the pad frame. To decrease voltage drop along the power ring, multi power pads are used for $VDDA$ and $VDDH$, and low voltage power pads needed to be placed into the high voltage domains. According to the design rule, substrate cutters, which also occupy some area in pad frame, have to be used between different voltage domains.

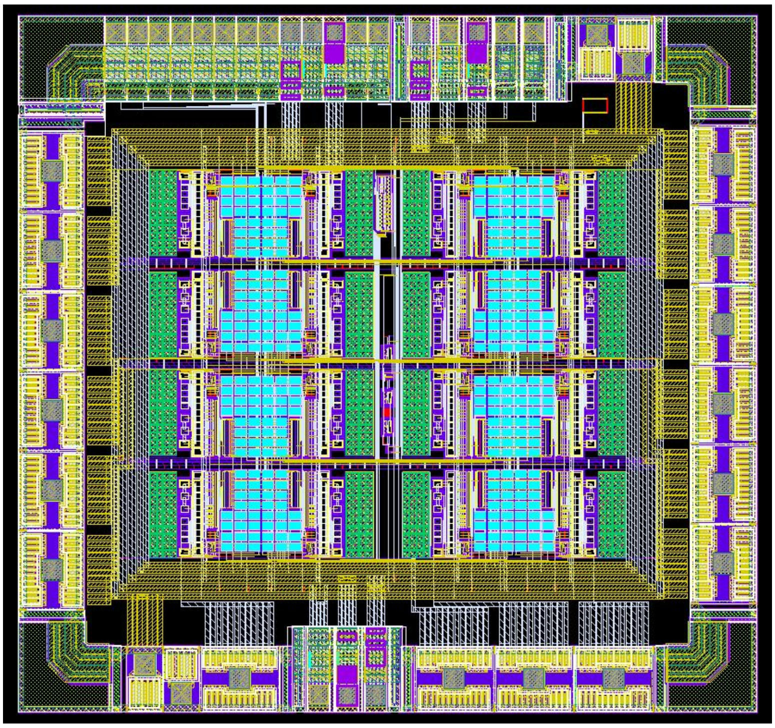


Fig. 4.14: Layout of the high voltage DAC array for tunable antenna array

In chapter 3, the chip size of the proposed single high voltage *DAC* is $3.5\ mm^2$. Comparing with it, the layout of this design is more compact. With a 16-channels high voltage *DAC* array and a simple digital controller, the layout size of "Taurus" including pad frame is only $10.88\ mm^2$ ($3.2mm * 3.1mm$).

In our previous work, an external *HV* switch array has to be used for driving antenna array. It has huge off capacitance of $192\ pF$ for 16 channels and greatly decreases the slew rate of the amplifier. With this configuration driving voltages on multi-channel can not be synchronously refreshed. In the worst case (from $0\ V$ to $120\ V$), it takes $37\ ms$ for 16 channels to achieve required voltage. The high voltage *DAC* array presented in this paper can drive 16 channels of the antenna array and refresh the 16 driving voltages synchronously. In the worst case, it only takes $1.6\ ms$ for 16 channels to reach $120\ V$. Comparing with our previous work, the switching time is 23 times shorter. The post-layout simulation is carried out with a load capacitance of $20\ pF$ for each channel by sweeping the input code from 0 to 255. The simulation result is shown in Fig. 4.15.

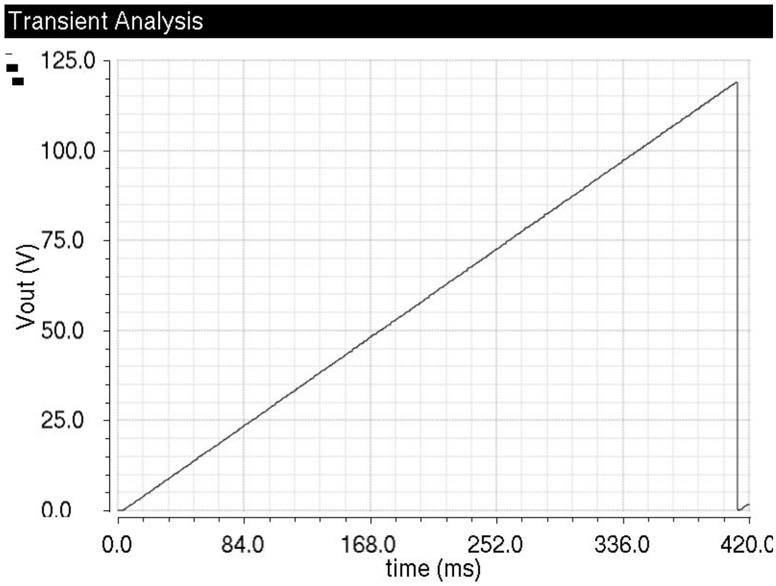


Fig. 4.15: Output voltage of one channel in the high voltage DAC array in post-layout simulation result.

Because of the parasitics, mismatch and process variations, and the voltage drop along the power ring, each *HV DAC* in this high voltage controller has different performances. Based on the simulation result, the important static characteristics (*INL* and *DNL*) and offset errors are given in Tab. 4.1.

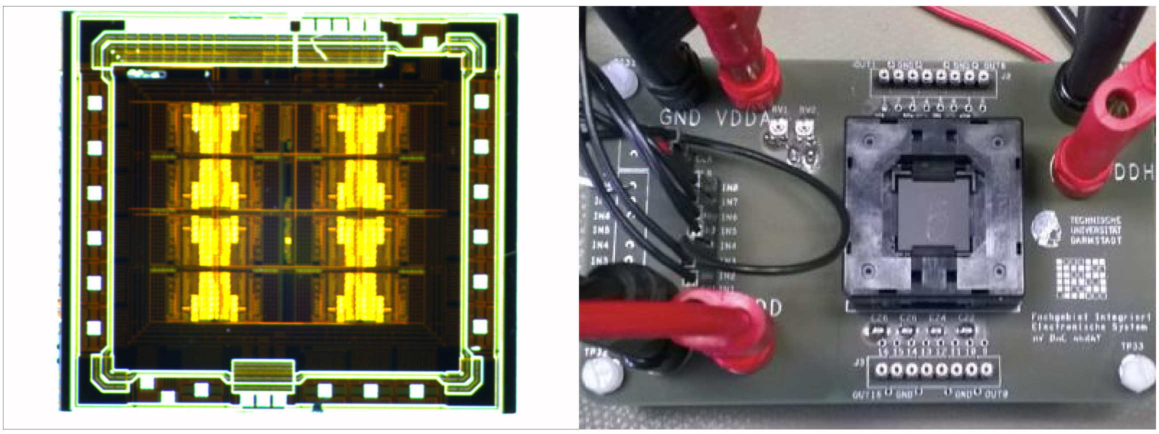
The maximum *INL* is $0.38\ LSB$ and the maximum *DNL* is $0.34\ LSB$. This result is based on the experimental test of one chip. Because of process and mismatch variation, each chip could have performance variations which will be discussed in the section 4.4.

Tab. 4.1: Post-layout simulation result of "Taurus"

	INL(LSB)	DNL(LSB)	Offset(mV)
DAC1	0.35	0.32	105
DAC2	0.37	0.34	103
DAC3	0.34	0.33	103
DAC4	0.33	0.30	105
DAC5	0.28	0.25	98
DAC6	0.35	0.31	99
DAC7	0.34	0.30	98
DAC8	0.29	0.25	98
DAC9	0.30	0.26	97
DAC10	0.33	0.28	98
DAC11	0.34	0.28	97
DAC12	0.32	0.25	96
DAC13	0.34	0.30	104
DAC14	0.35	0.32	101
DAC15	0.35	0.31	102
DAC16	0.38	0.33	104

4.4 Experimental Results for "Taurus"

The circuit design was fabricated and tested by *AMS* foundry in 2013. It was amounted in *QFN* package. The chip photos are shown in Fig. 4.16.



(a) (b)

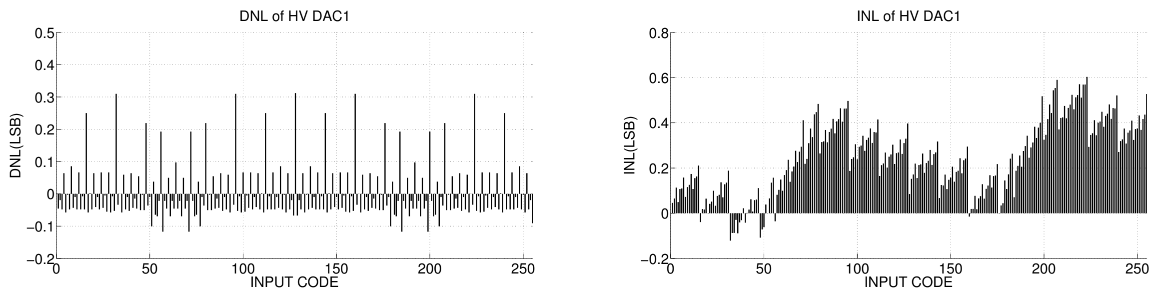
Fig. 4.16: The chip photo under microscope and the packaged ASIC

4.4.1 Measurement Result

A PCB board is designed for testing the chip. To avoid the interference, the ground is separated into three parts, high voltage region, low voltage analog region and digital region. The schematic and layout of the PCB board are shown in Appendix D.

Experimental *INL* and *DNL* are determined based on the measured output voltage. Each *HV DAC* has different *INL*, *DNL*, offset, and gain error as shown in Fig. 4.14. For each *HV DAC*, *INL* and *DNL* are calculated by sweeping the input code. In this figure, x-axis shows the input code from 0 to 255, and y-axis is the *INL* or *DNL*. For the 16 *HV DACs* on chip, the maximum *DNL* happens with the input code of 128 as the most significant bit being switched. The maximum *INL* of each *HV DAC* appears with different input code. For *HV DAC13*, it appears with the input code of 0 caused by a huge offset error. For *HV DAC8*, the maximum *INL* occurs with the last input code where has the largest accumulated error.

Both layout and mismatches during fabrication could lead to the performance variation. Normally, on chip resistance has maximum 30% variation. Even all resistors are drawn in the same shape and direction, the mismatch still exists and could cause output error. As shown in Fig. 4.7, the resistors in feedback loop are $0.1\ M\Omega$ and $5.9\ M\Omega$. Even 5 resistors of $0.5\ M\Omega$ are used in parallel to implement the resistance of $0.1\ M\Omega$, the process variation could still result in a huge variation of the resistors' ratio in the feedback loop. Since the chip area is relative large, the location of each *HV DAC* could also has impact on the performance. *HV DACs*, which are close to the power pads, have better performance. On the contrary, the performance of *HV DACs* placed in corners are relative worse because of the voltage drop along the power ring. As shown in this figure, *HV DAC1*, *HV DAC4*, *HV DAC13* and *HV DAC16*, which are placed far from the power pad and the regulator to generate the reference voltage, have worse *INL* and *DNL* than other *DACs*. Each *HV DAC* has different performance, even the chip layout is symmetrical. Besides the voltage drop across the metal line, the process and mismatch variation such as threshold voltage variation plays a role as well. Therefore, the maximum *INL* (*HV DAC13*) in this figure is a combination of the errors caused by these reasons.



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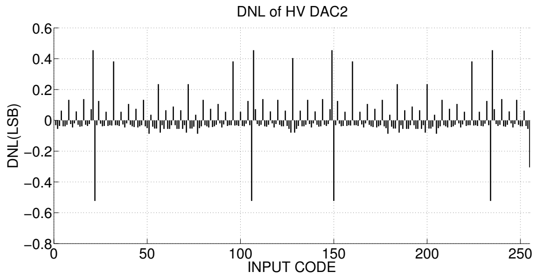
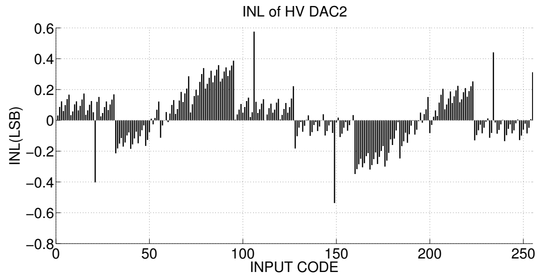
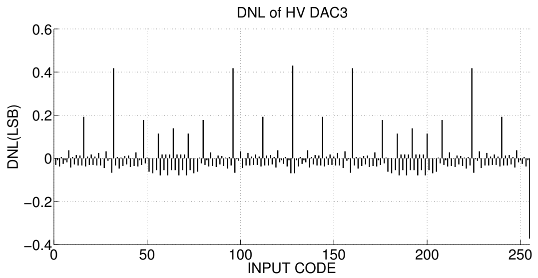


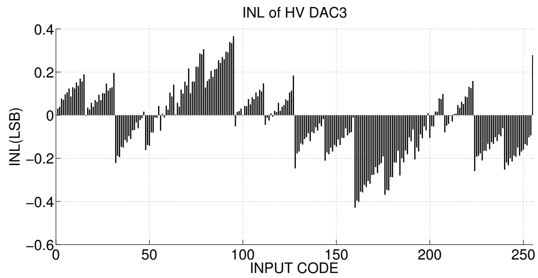
(5)



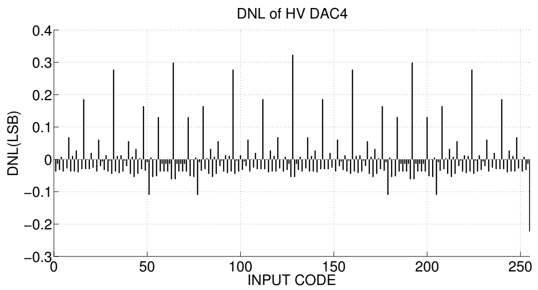
(6)



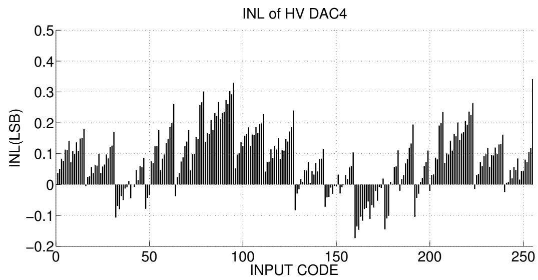
(7)



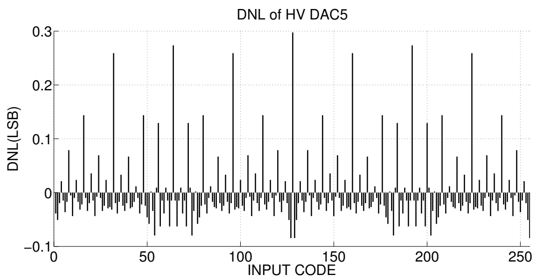
(8)



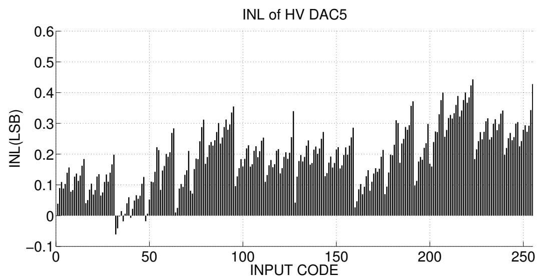
(9)



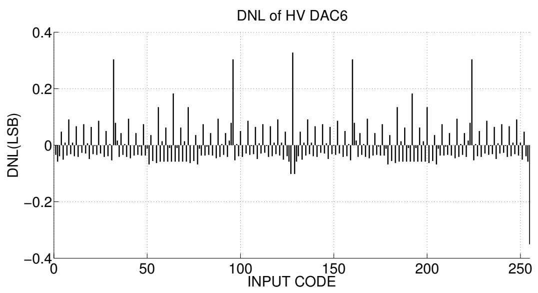
(10)



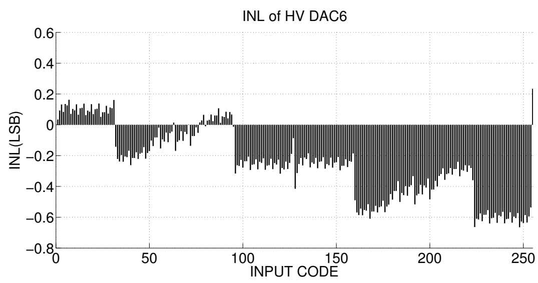
(11)



(12)



(13)



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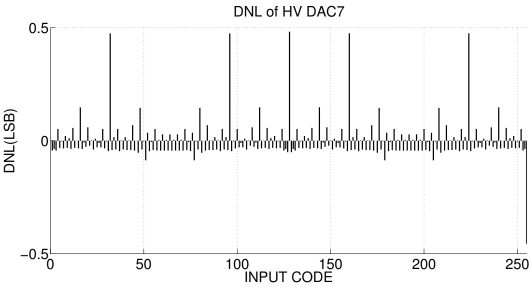

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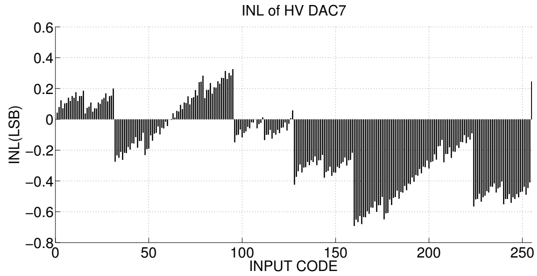

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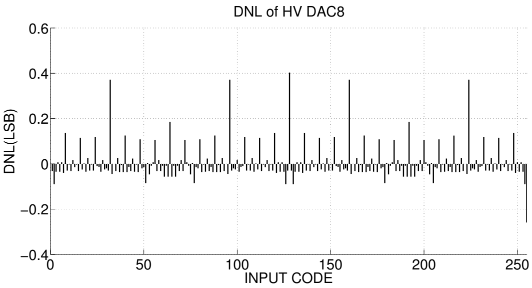

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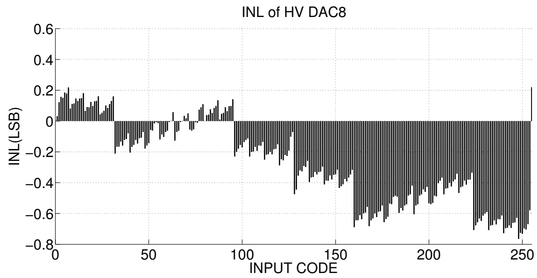

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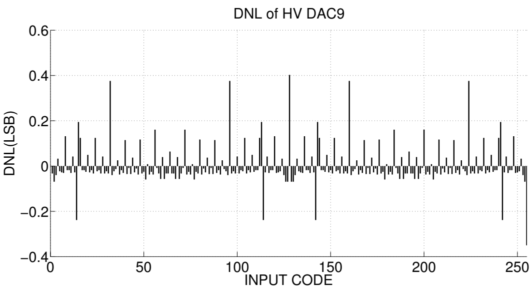
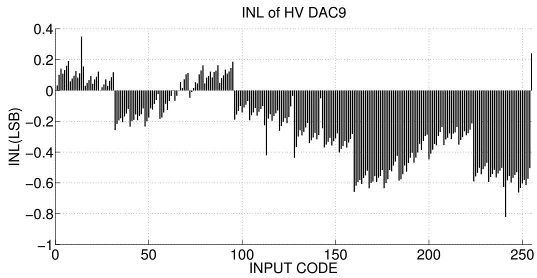
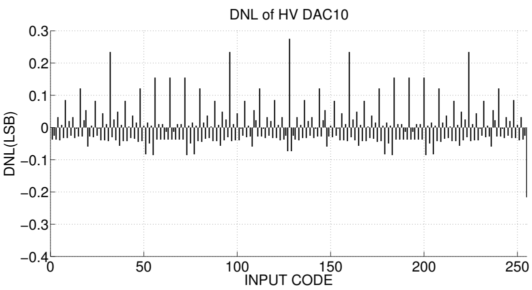


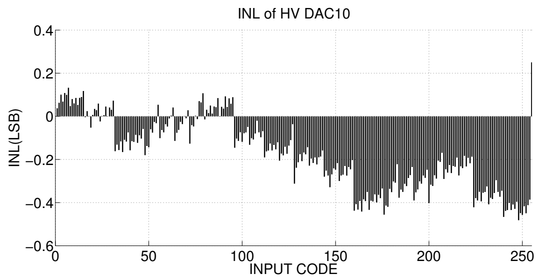
(31)



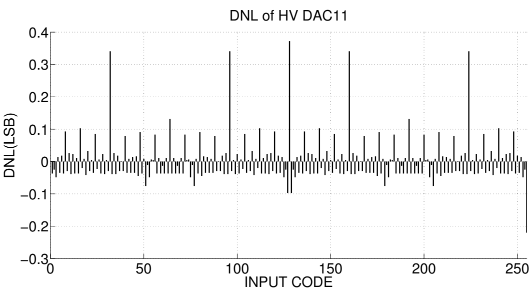
(32)



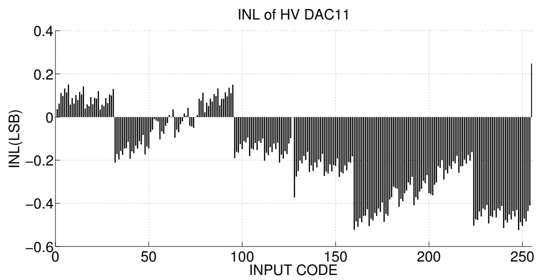
(33)



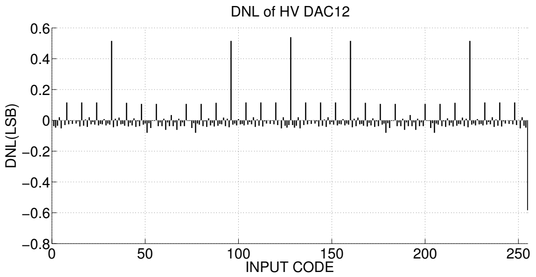
(34)



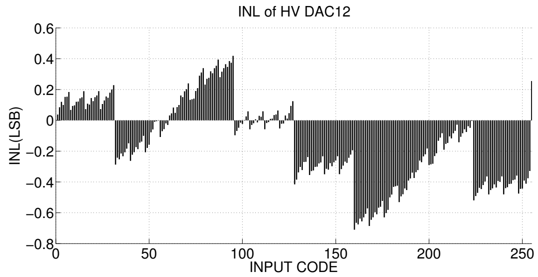
(35)



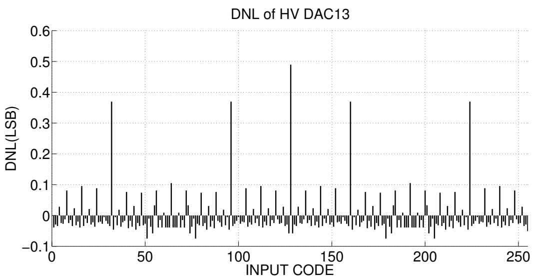
(36)



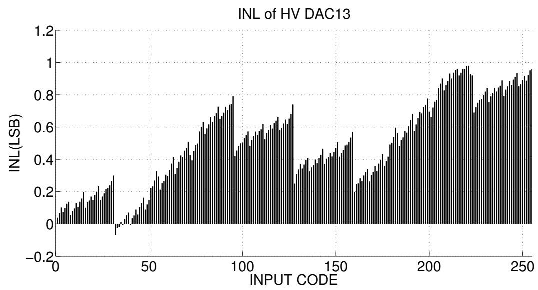
(59)



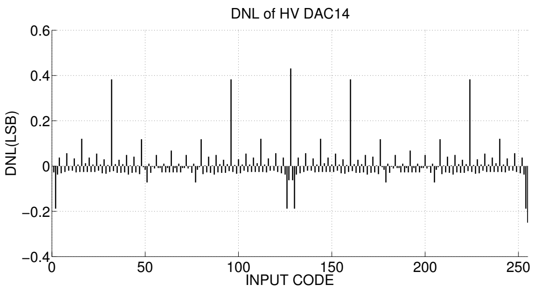
(60)



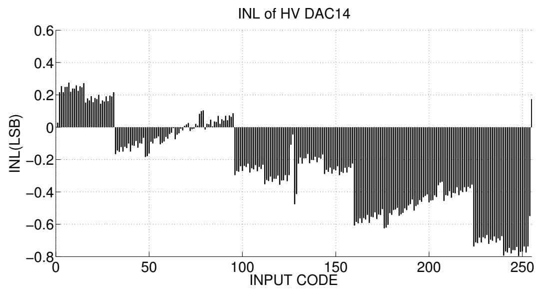
(61)



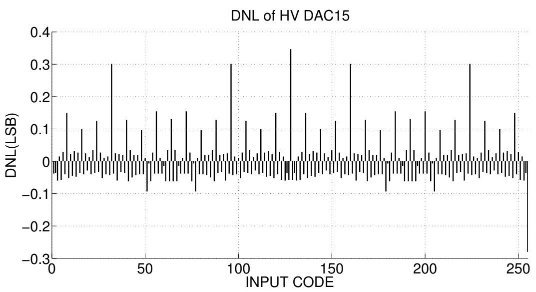
(62)



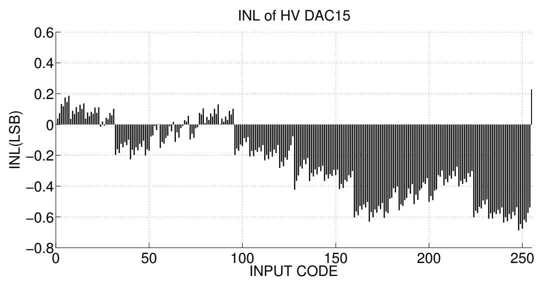
(63)



(64)



(65)



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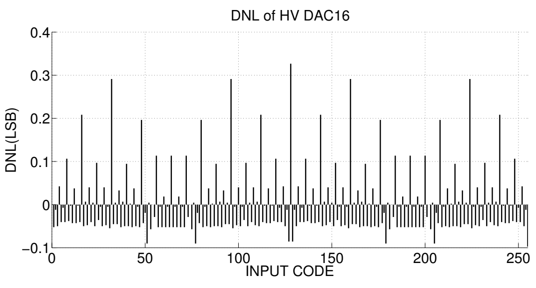

(67)

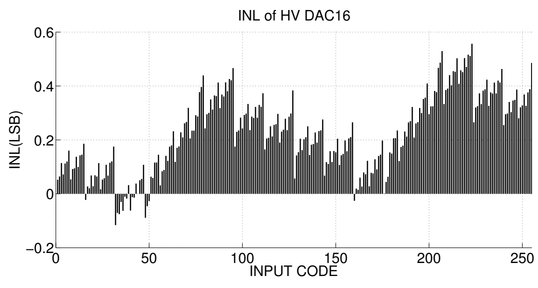

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Fig. 4.14: INL and DNL of 16 HV DACs

To show the performance of the chip, the measurement results of all *HV DACs* are summarized in Tab.4.2. The maximum *INL* is $0.98\ LSB$ (*HV DAC13*), and the maximum *DNL* is $0.58\,LSB$ (*HV DAC12*). The maximum *INL* comes from the offset as the input code being zero. The maximum gain error is $1.5\ LSB$. This result is based on the experimental test of one chip. Because of process and mismatch variation, each chip could have performance variations. According to the measurement of the samples, *INL* and *DNL* of all tested chips are smaller than $1\ LSB$ which means it can fulfill the accuracy requirement of the application. The measurement result proves the feasibility of using the proposed circuit topology to provide the required high voltage of tunable devices.

Tab. 4.2: Measurement result of "Taurus"

	INL(LSB)	DNL(LSB)	Offset(mV)
DAC1	0.60	0.31	221
DAC2	0.56	0.52	129
DAC3	0.42	0.43	115
DAC4	0.33	0.32	142
DAC5	0.44	0.30	178
DAC6	0.65	0.32	97
DAC7	0.68	0.47	103
DAC8	0.75	0.40	91
DAC9	0.80	0.40	100
DAC10	0.47	0.26	104
DAC11	0.51	0.38	103
DAC12	0.70	0.58	106
DAC13	0.98	0.48	417
DAC14	0.80	0.43	90
DAC15	0.67	0.38	95
DAC16	0.56	0.32	205

Chapter 5

Application of the ASICs as A High Voltage Driver in Communication Systems

Contents

This chapter introduces a demonstrator to use the proposed ASICs as a voltage driver for tunable devices in communication systems. The description and discussion are based on my own publication [NSGRH14].

5.1 Background

5.1.1 Motivation

In mobile and satellite communication systems, modern devices are required to support different standards such as *LTE*, *WIFI*, *Bluetooth* and *3G* under variable environmental conditions. A common solution to operate in different frequency bands and achieve the multi functionalities is to use multiple modules in RF frond-end of the communication systems. In this way, the hardware complexity will be greatly increased and the RF Frond-end becomes difficult to be integrated. For some mobile devices, the hardware size and integration density is not acceptable.

As introduced in previous chapters, to cope with this hardware increase, a better solution is to use reconfigurable microwave components to achieve multi-band capability. This can be realized e.g. by applying semiconductor, micro-electromechanical systems and functional materials such as liquid crystal. This kind of components changes its characteristics to reconfigure the architecture and to offer multiple services within the same RF chain or to compensate any emerging mismatch under changing condition. Considering the reliability and linearity, most research focus on the functional materials which require high tuning voltage. For example, *BST* has tuning voltage dependent electromagnetic properties and require a maximum biasing voltage above $90\ V$. If the high voltage controller can be implemented as a chip, it will be much easier to be integrated into hand-held devices than a discrete circuit.

5.1.2 Tuning Techniques

To support multiple frequency bands and overcome the changing environment impacts, two tuning techniques are used in this kind of flexible systems. One technique is to use switches connected to capacitors, inductors or grounded in series or shunt to the antenna. Different impedance can be applied to the antenna matching network by changing the switch state to shift frequency to what we expect. Although this method can improve $S11$ and system efficiency, it can not increase the antenna radiation efficiency with the fixed antenna feeding structure. The other solution is to use reconfigurable component in antenna structure to improve the antenna radiation efficiency [YWY14].

The theory and analysis method of designing impedance matching are well-established [SF96a, SF96b, SLL+07]. π and T type networks can be designed with a desired specification such as Q value, and other practical factors can also be taken into account in simulation.

5.2 Demonstrator of the Applications

To prove the concept proposed in this thesis, a demonstrator consists of a charge pump, two proposed ASICs and a dual-band antenna with a matching network was built. In Fig. 5.1, the block diagram of a proposed reconfigurable module is shown. The two high voltage DACs powered by a charge pump are used to control the tunable matching network module connected to the antenna. This system can be used in mobile devices such as mobile phone to provide good performance in different environmental conditions. For example, relocating the mobile phone close to body part or metallic surface could cause detuning case and increase the reflection parameter(S11) of the antenna. The proposed HV DACs can be used to provide a high bias voltage with a voltage step smaller than $0.47V$ for the matching network, which is built by using functional material, to compensate the detuning and mismatch. Since the proposed system can powered by battery, it will dramatically decrease the hardware size of the mobile devices.

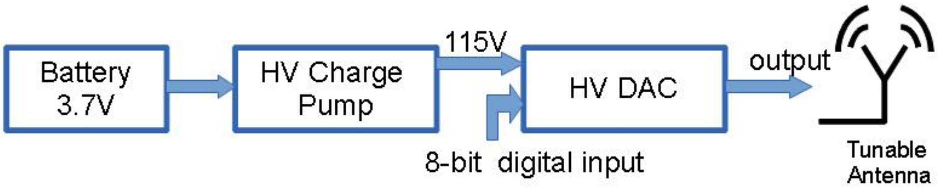

Fig. 5.1: Structure of demonstrator

As an important characteristic of the tunable matching network (*TMN*), it can be found that the relative permittivity of the *BST* layer is $\epsilon_{var} = 410$. Furthermore, the *TMN* module operates at a center frequency of $1.9\ GHz$ and can be tuned from $0\ V$ to $90\ V$, and thus, varying its capacitance from $0.31\ pF$ to $0.22\ pF$. It can be seen in the demonstrator in Fig. 5.2, the reference applied feeding voltage is performed by a $3.7\ V$ battery in order to generate a high voltage up to $120\,V$. Then both high voltage *DACs* are used to provide the required voltage in order to reconfigure the matching network, and thus, to compensate any detuning or mismatching of the antenna.

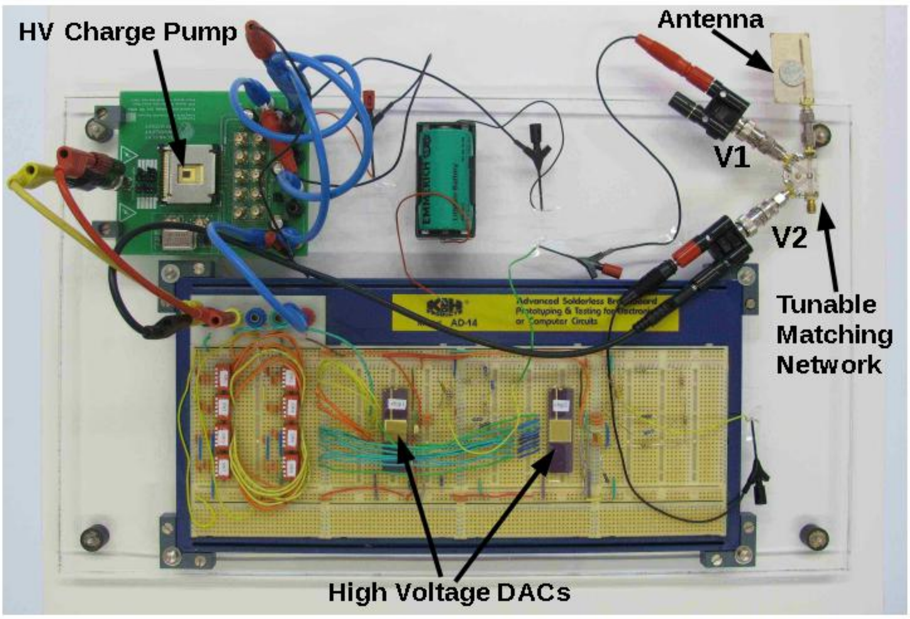

Fig. 5.2: Demonstrator

5.3 Measurement Result of the Demonstrator

S-parameters describe the input-output relationship between terminals in an electrical system. In practice, the most commonly quoted parameter with regard to antennas is $S11$. It describes how much power is reflected from the antenna. In ideal case, $S11$ equals 0 which means all power is transmitted. When $S11$ equals $-3\ dB$, the reflection power ratio equals 10%. Normally, if $S11$ is lower than $-10\ dB$, the attenuation of the antenna is acceptable. In Fig. 5.3, measurements of the $S11$ input reflection parameter for different voltage values of the *TMN* are shown. The input reflection parameter depends on matching degree of the antenna. The capacitors implemented by using *BST* can change their capacitance values while different biasing voltages provided by the proposed high voltage *DAC*. The matching degree is improved by changing capacitance values in the *TMN*. According to our measurement result, the $S11$ parameter is greatly improved by changing biased voltages. As shown in this figure, in the best case, the $S11$ parameter can be reduced to $-25\ dB$, which means accurate capacitance values are achieved using biasing voltages provided by the high voltage *DAC*.

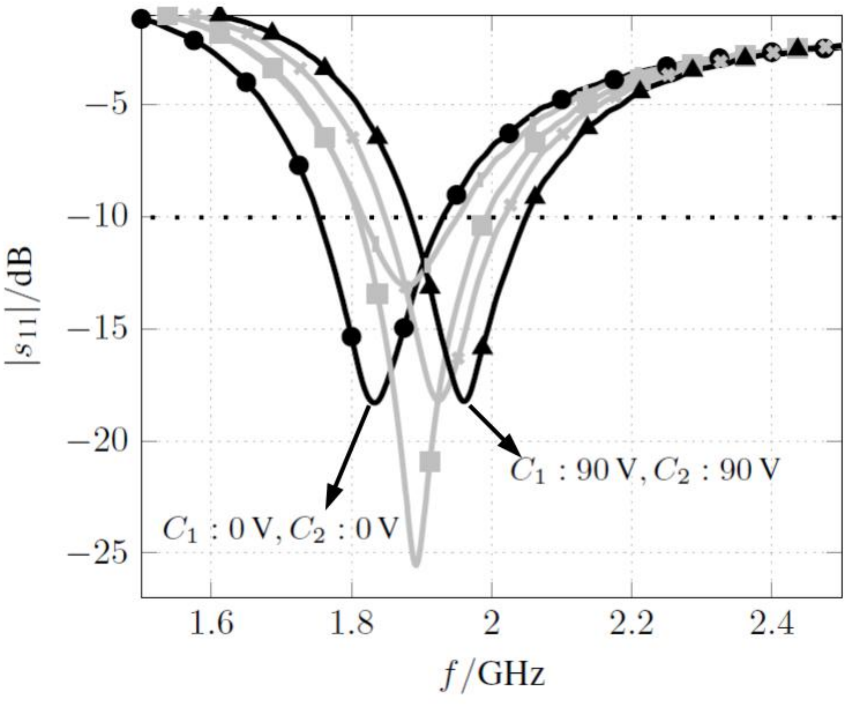

Fig. 5.3: Measured input reflection of the TMN module for different capacitance values biased from 0 V to 90 V

Fig.5.4 shows the measurement result of the $S11$ parameter while locating the antenna close to metallic surfaces or near to the head. Huge performance improvement can be obviously observed under matching cases. Strong mismatch in the lower band of the antenna is clearly observed by the influence of the detuning. In the upper band this influence is almost negligible in all cases. The detuning has a big impact on the center frequency and reduces the reflection amplitude to value worse than $-10\ dB$. In order to fix the mismatch of the lower band, different voltage of the matching network were applied by using the *ASICs*. Then, the center frequency of the antenna is stabilized at the desired one ($1.9\ GHz$) with reflection amplitude around $-25\ dB$. Furthermore, due to the detuning compensation, both bands exhibit a narrower bandwidth. For the lower band, the antenna bandwidth is reduced from $420\ MHz$ to $110\ MHz$, and for the upper band from $640\ MHz$ to $270\ MHz$. The antenna becomes more selective by 74% and 57%, respectively.

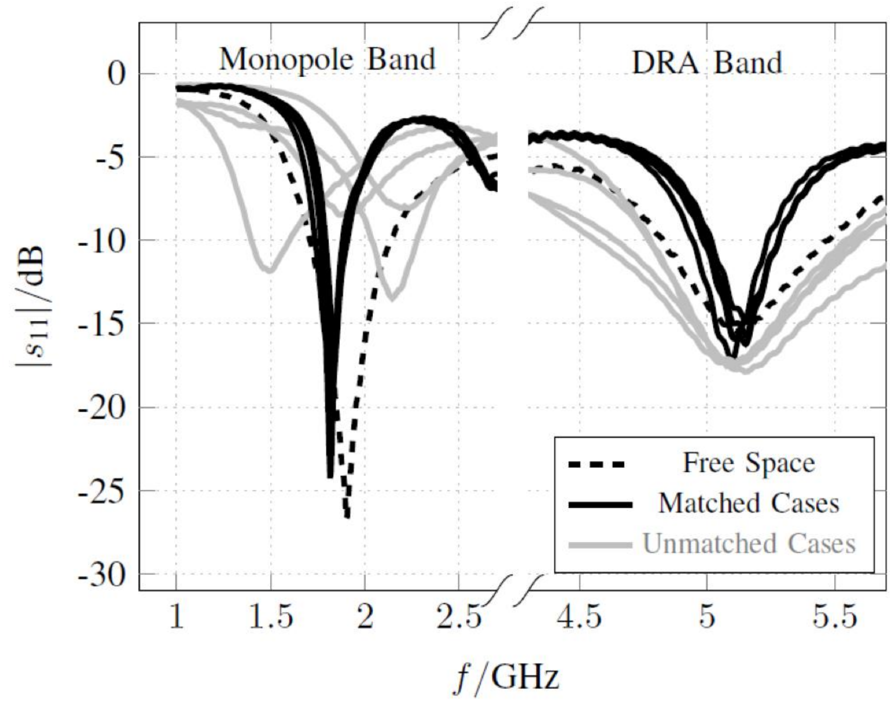

Fig. 5.4: Measured input reflection for different evaluated cases of the DRA input impedance.

Since the input impedance of the matching network is pure capacitive, it will not change the load resistance of the *HV* amplifier in the proposed *HV DACs*. The influence on the statistic performance of the *HV DAC* can be negligible. In this application, the maximum INL and maximum DNL of the *DAC* are $0.22\ V$ and $0.18\ V$, respectively. They can fulfill the required accuracy($0.5\ V$) of the biasing voltage for the matching network. Normally, the input capacitance of antenna is $10-20pF$, which is the bottleneck for the speed provided by driving circuits. But in this demonstrator, the input capacitance is much smaller than the one used in Sec. 3.4 for measurement. Therefore, the speed is not limited by the load capacitance anymore. It can be charged to the maximum biasing voltage of $90\ V$ in $3\mu S$.

5.4 Conclusion

This chapter describes a demonstrator for a reconfigurable dual-band antenna with a matching network and proved the feasibility of the design concept in this thesis. The high voltage *DACs* are used to provide individual biasing voltage with $0.47\ V$ voltage step for different ports of the matching network. The high biasing voltage of the matching network are provided by the proposed *HV DACs*. Due to the low current consumption from the high voltage power supply, the *HV DAC* can be powered by a high voltage power supply generated by a charge pump from a battery. In this way, the system can be powered only by a battery without any extra high voltage power supply.

By measuring the demonstrator, it has been proved that the high biasing voltage and the required voltage accuracy can be fulfilled by using the proposed *HV DACs*. The functional materials are also used in other modules in mobile and communication systems to achieve new multi-band and multi-condition capabilities. The maximum required voltage and the required voltage accuracy are the same as this demonstrator. Therefore, it has been proved that the high voltage requirement to offer multi-band functionality in these systems can be fulfilled by high voltage technologies and System-on-Chip concepts. It has also been proven that the complexity of communication systems with tunable components made of voltage dependent materials can be significantly reduced by using high voltage *ASICs*. Thus, combining with functional materials, high voltage *ASICs* can be a new solution to achieve the multi-band requirements without extra hardware and cost.

Chapter 6

Conclusion and Outlook

Contents

6.1 Conclusion

The signals in the real world are not digital and can not be presented as low and high levels, or zeros and ones. To process these analog signals within a range of voltages or currents, the data converters (*ADC* and *DAC*) are invented to build the interface between the real world and a digital processor. The purpose of the digital to analog converter (*DAC*) is to convert a digital data into a signal in analog domain which is required by the next stage in the system. Whether a motor driver, or an LED display, or an audio amplifier exists in the system, the final signal must be in analog domain. Thus, *DAC* is used as an interface to transfer a digital signal into a accurate analog value, and becomes an important circuit block in the past decades.

Compared to conventional *DACs*, *High Voltage DAC* design is relatively new in the field of *ASIC* design. It is mostly used for medical applications, audio and video applications. For *HV ASIC* design, more issues have to be considered such as more parasitics in high voltage technologies, additional high voltage power supply, high power consumption and relatively large size of high voltage devices.

In this dissertation, two high voltage *ASICs* are designed in *AMS H35* for tunable antenna arrays in communication systems, and they can be powered by an on-chip DC-DC converter which can generate $120\ V$ from a battery. Both *ASICs* are simulated, implemented and experimentally tested.

The first *ASIC* ("Aries") was implemented and measured in 2012. It is a high voltage *DAC* designed with segmented topology consisting of a low voltage *DAC* and a *HV*

Tab. 6.1: Performance comparison of the ASICs with previous designs.

	[HC12]	[SMP05]	Aries	"Taurus"
Technology	$0.25\mu m$	$0.8\mu m$	$0.35\mu m$	$0.35\mu m$
Output Range(V)	0-60	0-300	0-115	0-120
Resolution	10-bits	6-bits	8-bits	8-bits
DNL(LSB)	0.003 (simulated result)	0.16 (simulated results)	0.38 (measured result)	0.52 (measured result)
INL(LSB)	0.28 (simulated result)	0.18 (simulated result)	0.48 (measured result)	0.98 (measured result)
Chip Area(mm^2)	2.9279	not available	3.5	10.88
Power(mW)	not available	not available	18	120

Miller-compensated Amplifier to boost up the output of the *LV DAC* to the required high voltage range. It can provide output voltage from $0\ V$-$115\ V$ with maximum *INL* of $0.48\ LSB$ and the maximum *DNL* of $0.38\ LSB$, respectively. The current consumption from the *HV* power supply is less than $100\ \mu A$, and the power consumption of the chip is $18\ mW$. It is possible to be used with external switches to provide multiple individual voltages for different channels in antenna arrays. The total size of this *ASIC* ("Aries") is $3.5\ mm^2$.

The second *ASIC* ("Taurus") was implemented and measured in 2013. It is a high voltage controller with 16 *HV DACs* and a simple digital controller. Several circuit blocks in the first design are reused and modified to build "Taurus". In this version, the output voltage range is expanded to $0V$-$120V$ which is the maximum safe operation voltage provided by the technology. Since 16 *HV DACs* are available on chip, the external switches can be eliminated as driving multiple channels. Thus, the parasitic capacitance at the input node of the antenna is significantly reduced, and the speed to reach the expected voltage is greatly improved. Because of the process and mismatch variations during fabrication, each *HV DAC* on this chip has different performance. The worst measurement result is taken as the measured specification. The maximum *INL* and *DNL* are $0.98\,LSB$ and $0.52\ LSB$, respectively. The current consumption from the *HV* power supply is $1.28\ mA$, and the total power consumption of the chip is $120\ mW$. The chip size of "Taurus" is $10.88\ mm^2$.

The comparison between the proposed *ASICs* and other published *HV DAC* designs are shown in Tab. 6.1.

Besides the measurement result, a demonstrator is built to prove the feasibility of integrating *HV AISCs* into portable devices for driving tunable RF components to achieve the multi-band functionality and come over the impact of changing environment conditions. Compared to the traditional solution, which uses multiple modules in RF Front-end, integrating reconfigurable devices and *HV AISCs* into hand-held devices greatly reduces the hardware size and complexity. For portable devices powered by battery, it is also a better solution to apply required biasing voltage with *HV ASICs* which can operate with a high voltage power supply generated by a DC-DC converter.

6.2 Outlook

Based on the measurement result of the proposed *ASICs*, further work can focus on improving the performance such as reducing gain error difference between *HV* channels on one chip and eliminating huge offset error. These performances can be improved with offset cancellation techniques and better layout strategies. Because of the worse characteristics of the devices in this high voltage technology, it is very difficult to achieve high resolution above 10-bits with R2R transistor only topology and current steering topology. Thus, in future the low voltage part has to be replaced by using *Delta-sigma DAC* which can relax the requirements on the analog part and reduce matching tolerances as higher resolution required.

Furthermore, *HV ASICs* can also be used in other applications such as medical devices and optical communication systems. For example, *VCSEL* in optical communication systems requires high driving voltage/current to generate signal with different wavelengths. Reusing the proposed topology and *HV ASIC* design methodology for other applications is another interesting work in the future.

Appendix A

Device Parameters and Layout of the first ASIC("Aries")

Tab. A.1: Device parameters in the proposed R2R transistors only DAC and high voltage amplifier

R2R transistor only DAC shown in Fig. 3.2	M1, M2,M3...M37	$8\mu m/5\mu m$
High Voltage Amplifier shown in Fig. 3.13	M9, M10	$26\mu m/1\mu m$
	M11, M12	$10\mu m/1\mu m$
	M13	$16\mu m/1\mu m$
	M14	$5\mu m/1\mu m$
	M15	$10\mu m/5\mu m$
	M16	$10\mu m/2\mu m$
	M7	$10\mu m/2\mu m$
	M8	$5\mu m/1\mu m$
	M3	$40\mu m/1\mu m$
	M4	$36.4\mu m/0.7\mu m$
	M2, M6	$20\mu m/1.2\mu m$
	M5	$12\mu m/2\mu m$
	M1	$108\mu m/2\mu m$

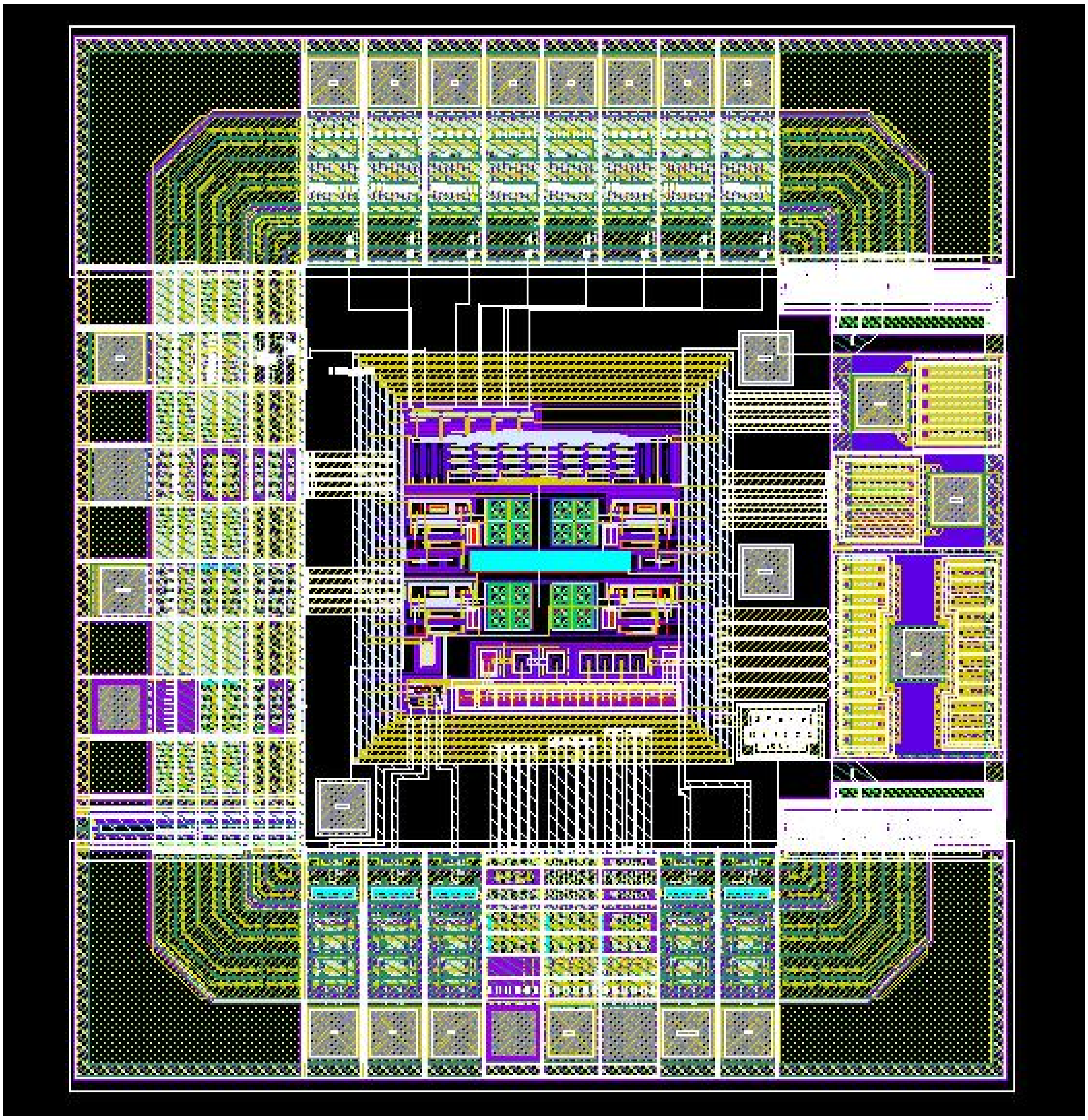

Fig. A.1: Layout of the high voltage digital to analog converter(”Aries”) for reconfigurable antenna array.

Appendix B

Device Parameters and Layout of the Second ASIC (”Taurus”)

Tab. B.1: Device parameters in the proposed low voltage current steering DAC and high voltage amplifier

<table>
<tr><td rowspan="4">Current Steering DAC shown in Fig. 4.6</td><td>(M1, M2), (M5, M6), (M12, M13)...(M57, M58)</td><td>$9\mu m/3\mu m$</td></tr>
<tr><td>M11...M40</td><td>$9\mu m/5\mu m$</td></tr>
<tr><td>M3, M7, M9, M14, M16...M53, M59</td><td>$10\mu m/0.5\mu m$</td></tr>
<tr><td>M4, M8, M10, M15, M17...M54, M60</td><td>$10\mu m/1\mu m$</td></tr>
<tr><td rowspan="13">High Voltage Amplifier shown in Fig. 4.10</td><td>M9, M10</td><td>$26\mu m/1\mu m$</td></tr>
<tr><td>M11, M12</td><td>$10\mu m/1\mu m$</td></tr>
<tr><td>M13</td><td>$15\mu m/1\mu m$</td></tr>
<tr><td>M14</td><td>$5\mu m/1\mu m$</td></tr>
<tr><td>M15</td><td>$10\mu m/5\mu m$</td></tr>
<tr><td>M16</td><td>$10\mu m/2\mu m$</td></tr>
<tr><td>M7</td><td>$10\mu m/2\mu m$</td></tr>
<tr><td>M8</td><td>$5\mu m/1\mu m$</td></tr>
<tr><td>M3</td><td>$40\mu m/1\mu m$</td></tr>
<tr><td>M4</td><td>$36.4\mu m/0.7\mu m$</td></tr>
<tr><td>M2, M6</td><td>$20\mu m/1.2\mu m$</td></tr>
<tr><td>M5</td><td>$12\mu m/2\mu m$</td></tr>
<tr><td>M1</td><td>$108\mu m/2\mu m$</td></tr>
</table>

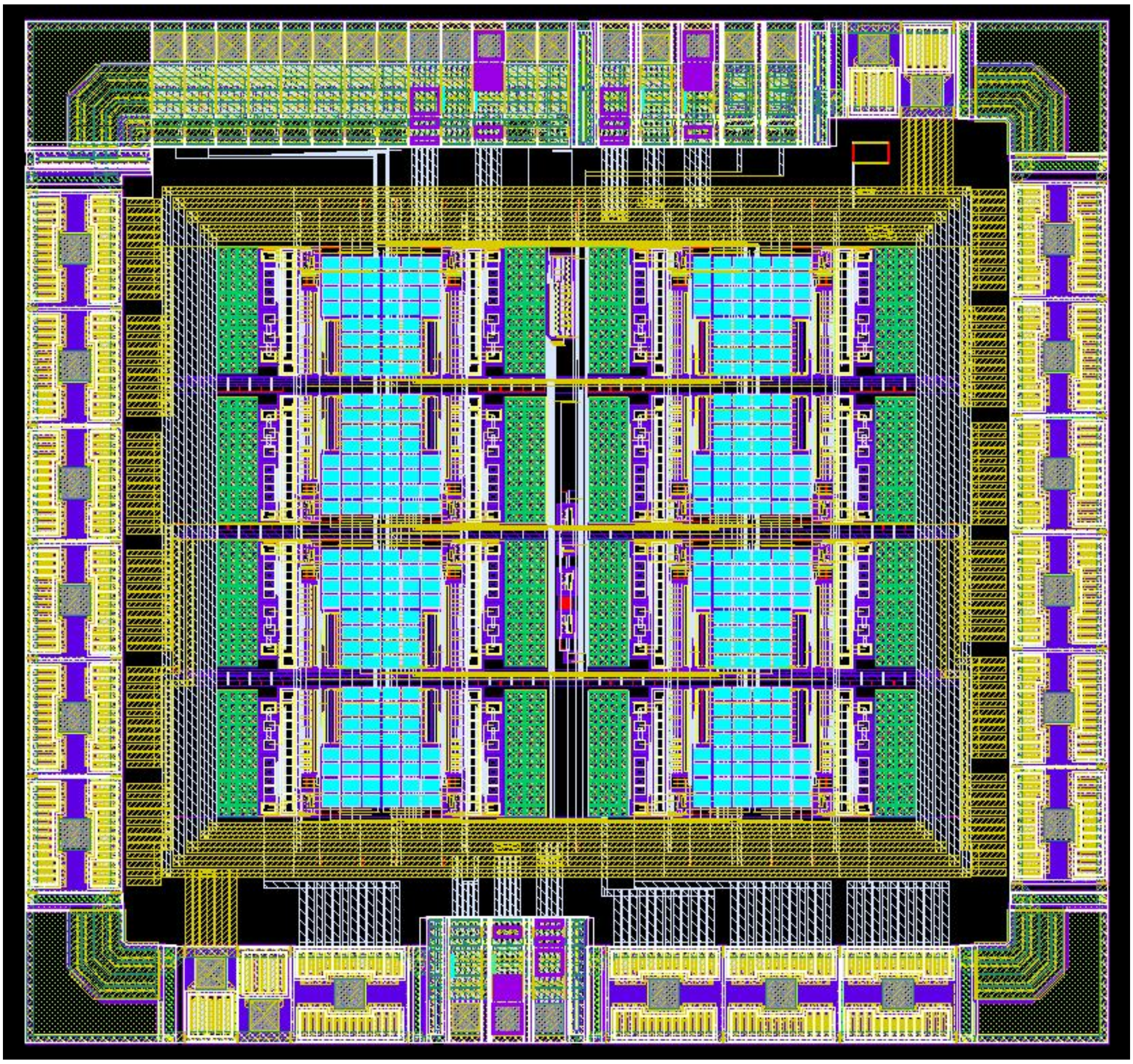

Fig. B.1: Layout of the high voltage controller with 16 high voltage DACs ("Taurus") for tunable antenna arrays

Appendix C

IC Package Information of ″Taurus″

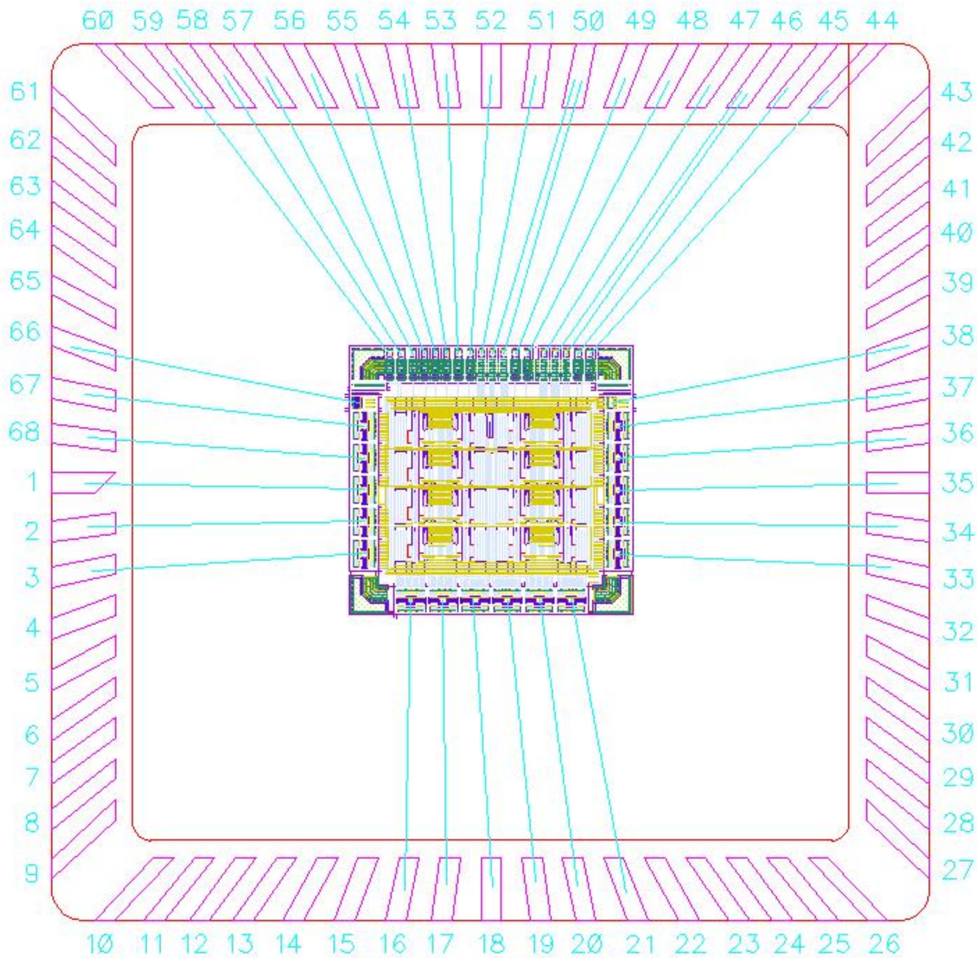

Fig. C.1: Bonding diagram of ″Taurus″

Tab. C.1: Pin list of ”Taurus”

Pin Nr	Type	Direction	Description
68	digital	in	CLK signal, 0/5V
69	digital	in	Clear signal, 0/5V
71	digital	in	VDDD, digital power supply, 5V
70	digital	inout	GNDD, digital ground, 0V
72-79	digital	in	In1-In8, 8-bits digital input, 0/5V
31	analog	in	VDDA, analog power supply, 5V
67	analog	in	VDDA, analog power supply, 5V
30	analog	inout	GNDA, analog ground, 0V
66	analog	inout	GNDA, analog ground, 0V
27	analog	in	VDDH, high voltage power supply, 120V
62	analog	in	VDDH, high voltage power supply, 120V
28	analog	inout	GNDH, high voltage analog ground, 0V
63	analog	inout	GNDH, high voltage analog ground, 0V
56	analog	out	Output1, output signal of HV DAC1, 0-120V
54	analog	out	Output2, output signal of HV DAC2, 0-120V
52	analog	out	Output3, output signal of HV DAC3, 0-120V
50	analog	out	Output4, output signal of HV DAC4, 0-120V
48	analog	out	Output5, output signal of HV DAC5, 0-120V
46	analog	out	Output6, output signal of HV DAC6, 0-120V
34	analog	out	Output7, output signal of HV DAC7, 0-120V
33	analog	out	Output7, output signal of HV DAC8, 0-120V
32	analog	out	Output9, output signal of HV DAC9, 0-120V
29	analog	out	Output10, output signal of HV DAC10, 0-120V
15	analog	out	Output11, output signal of HV DAC11, 0-120V
13	analog	out	Output12, output signal of HV DAC12, 0-120V
11	analog	out	Output13, output signal of HV DAC13, 0-120V
9	analog	out	Output14, output signal of HV DAC14, 0-120V
7	analog	out	Output15, output signal of HV DAC15, 0-120V
5	analog	out	Output16, output signal of HV DAC16, 0-120V

Appendix D

Design of Evaluation Board for "Taurus"

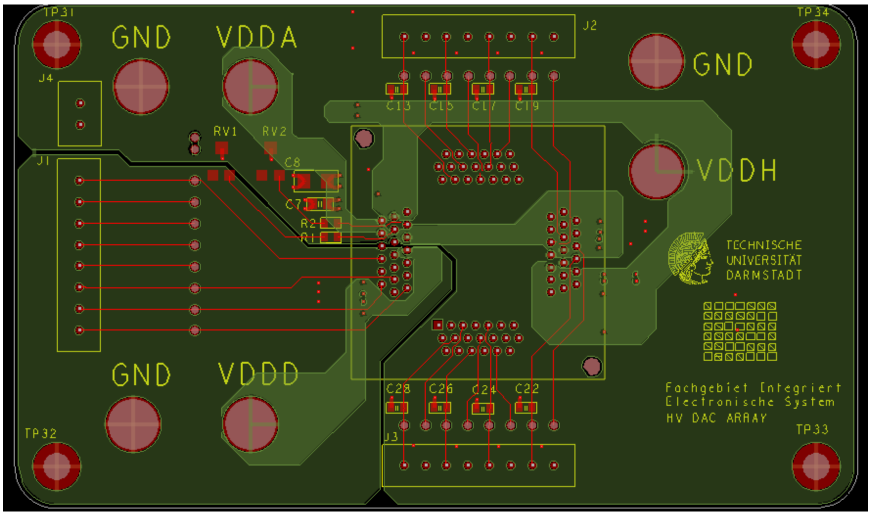

Fig. D.1: Top view of the evaluation board

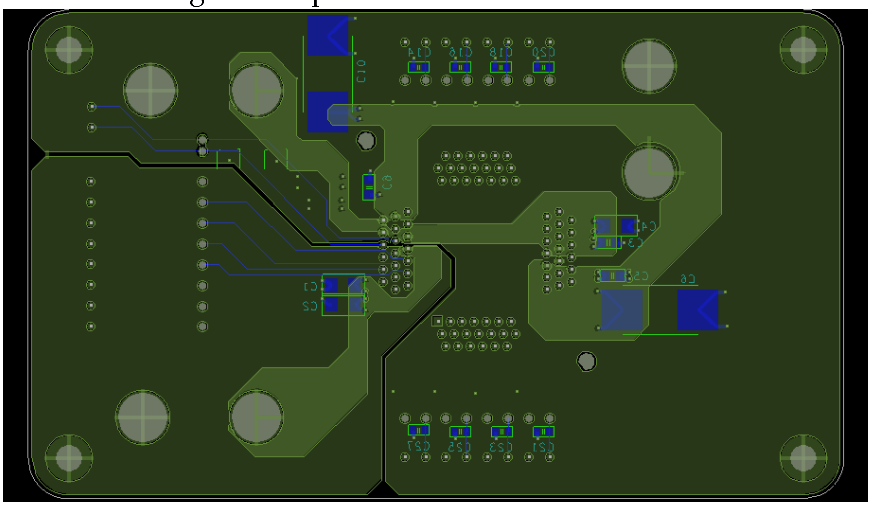

Fig. D.2: Bottom view of the evaluation board

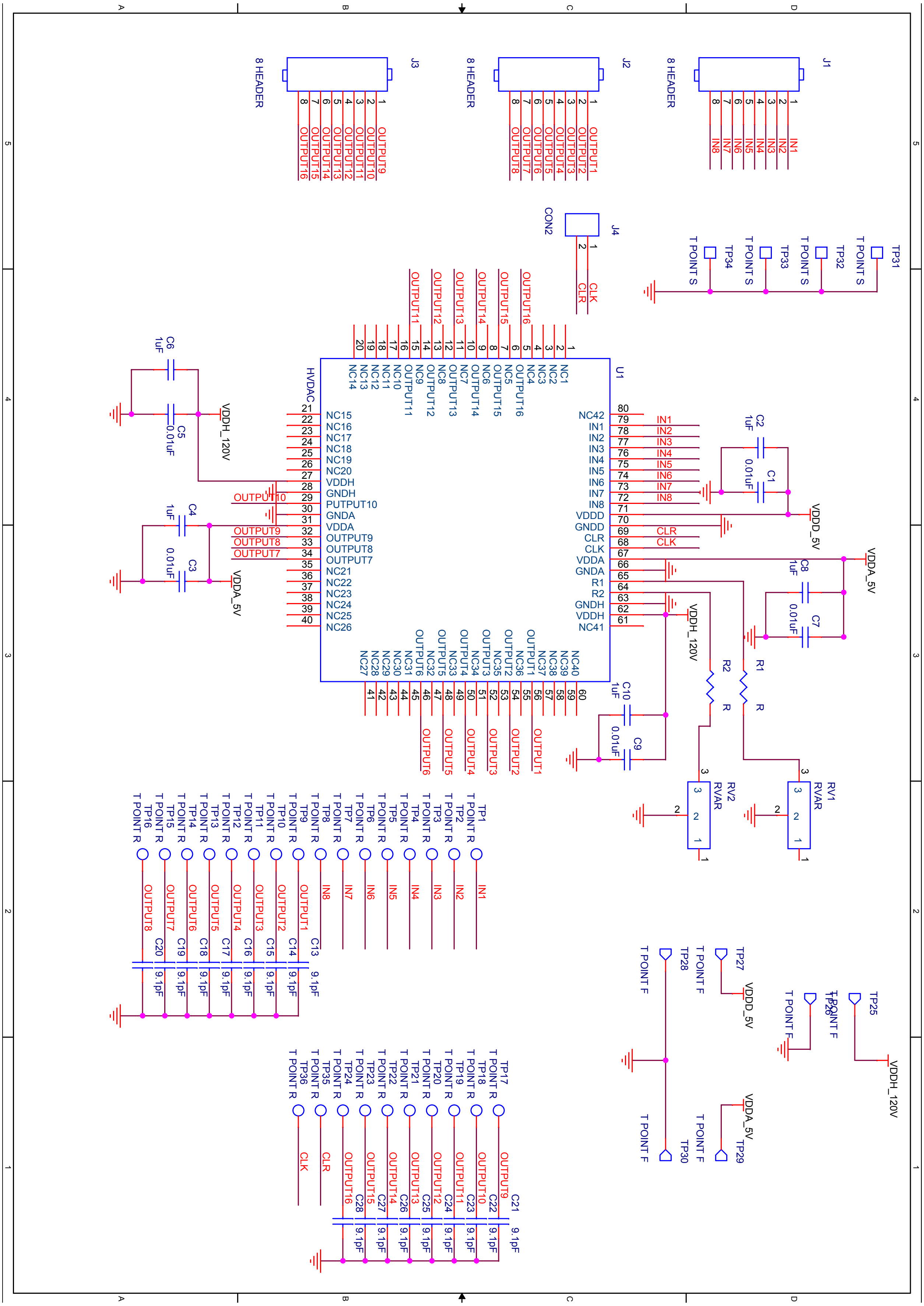

Fig. D.3: Schematic of the evaluation board for "Taurus"

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Supervised Theses

[1] A 10 bits binary weighted capacitor high voltage digital to analog converter in ams technology.

[2] Design of a digital front-end of 14 enob sigma-delta digital-to-analog converter in ams h35 technology.

[3] Design of a modulator for an 8 bit noise shaping adc with ams-h35 technology.

[4] Design of a rail to rail amplifier with offset cancellation technique.

[5] High voltage current controlled switch array for high voltage dac.

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